

# VIPA System 200V

**FM | Manual**

HB97E\_FM | RE\_250-1BA00 | Rev. 13/02

January 2013



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Conformity is indicated by the CE marking affixed to the product.

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## About this manual

This manual describes the System 200V Counter module FM 250 from VIPA. Here you may find every information for commissioning and operation.

### Overview

#### **Chapter 1: Basics and Assembly**

The focus of this chapter is on the introduction of the VIPA System 200V. Here you will find the information required to assemble and wire a controller system consisting of System 200V components.

Besides the dimensions the general technical data of System 200V will be found.

#### **Chapter 2: Hardware description**

Here the hardware components of the FM 250-1BA00 are described.

The technical data are at the end of the chapter.

#### **Chapter 3: Deployment**

This chapter provides information to the configuration and the various counter modes of the Counter module FM 250 are described.

**Objective and contents**

This manual describes the System 200V Counter module FM 250-1BA00 from VIPA. It contains a description of the construction, project implementation and usage.

This manual is part of the documentation package with order number HB97E\_FM and relevant for:

Product	Order number	as of state: HW
FM 250	VIPA 250-1BA00	01

**Target audience**

The manual is targeted at users who have a background in automation technology.

**Structure of the manual**

The manual consists of chapters. Every chapter provides a self-contained description of a specific topic.

**Guide to the document**

The following guides are available in the manual:

- an overall table of contents at the beginning of the manual
- an overview of the topics for every chapter

**Availability**

The manual is available in:

- printed form, on paper
- in electronic form as PDF-file (Adobe Acrobat Reader)

**Icons Headings**

Important passages in the text are highlighted by following icons and headings:



**Danger!**

Immediate or likely danger.  
Personal injury is possible.



**Attention!**

Damages to property is likely if these warnings are not heeded.



**Note!**

Supplementary information and useful tips.

## Safety information

### Applications conforming with specifications

The FM 250 is constructed and produced for:

- all VIPA System 200V components
- communication and process control
- general control and automation applications
- industrial applications
- operation within the environmental conditions specified in the technical data
- installation into a cubicle



### Danger!

This device is not certified for applications in

- in explosive environments (EX-zone)

### Documentation

The manual must be available to all personnel in the

- project design department
- installation department
- commissioning
- operation



### The following conditions must be met before using or commissioning the components described in this manual:

- Hardware modifications to the process control system should only be carried out when the system has been disconnected from power!
- Installation and hardware modification only by properly trained personnel.
- The national rules and regulations of the respective country must be satisfied (installation, safety, EMC ...)

### Disposal

**National rules and regulations apply to the disposal of the unit!**



# Chapter 1 Basics and Assembly

**Overview** The focus of this chapter is on the introduction of the VIPA System 200V. Here you will find the information required to assemble and wire a controller system consisting of System 200V components. Besides the dimensions the general technical data of System 200V will be found.

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## Safety Information for Users

### Handling of electrostatic sensitive modules

VIPA modules make use of highly integrated components in MOS-Technology. These components are extremely sensitive to over-voltages that can occur during electrostatic discharges.

The following symbol is attached to modules that can be destroyed by electrostatic discharges.



The Symbol is located on the module, the module rack or on packing material and it indicates the presence of electrostatic sensitive equipment.

It is possible that electrostatic sensitive equipment is destroyed by energies and voltages that are far less than the human threshold of perception. These voltages can occur where persons do not discharge themselves before handling electrostatic sensitive modules and they can damage components thereby, causing the module to become inoperable or unusable.

Modules that have been damaged by electrostatic discharges can fail after a temperature change, mechanical shock or changes in the electrical load.

Only the consequent implementation of protection devices and meticulous attention to the applicable rules and regulations for handling the respective equipment can prevent failures of electrostatic sensitive modules.

### Shipping of electrostatic sensitive modules

Modules must be shipped in the original packing material.

### Measurements and alterations on electrostatic sensitive modules

When you are conducting measurements on electrostatic sensitive modules you should take the following precautions:

- Floating instruments must be discharged before use.
- Instruments must be grounded.

Modifying electrostatic sensitive modules you should only use soldering irons with grounded tips.



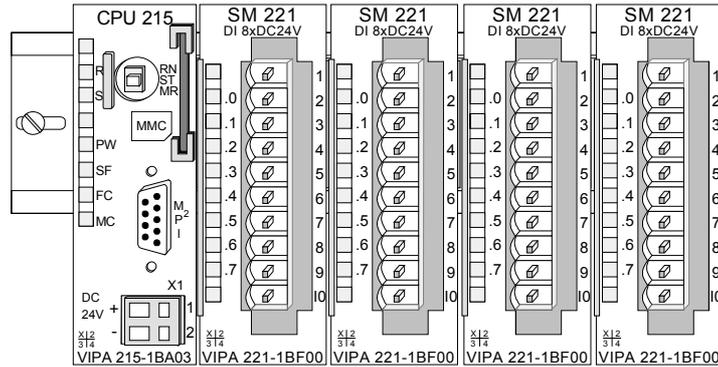
### Attention!

Personnel and instruments should be grounded when working on electrostatic sensitive modules.

# System conception

## Overview

The System 200V is a modular automation system for assembly on a 35mm profile rail. By means of the peripheral modules with 4, 8 and 16 channels this system may properly be adapted matching to your automation tasks.

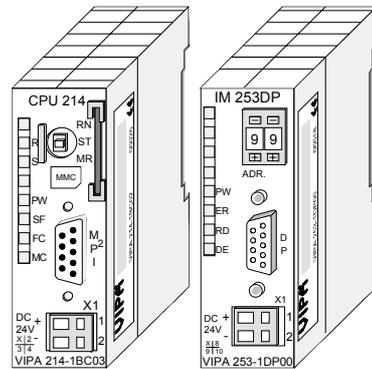


## Components

The System 200V consists of the following components:

- Head modules like CPU and bus coupler
- Periphery modules like I/O, function und communication modules
- Power supplies
- Extension modules

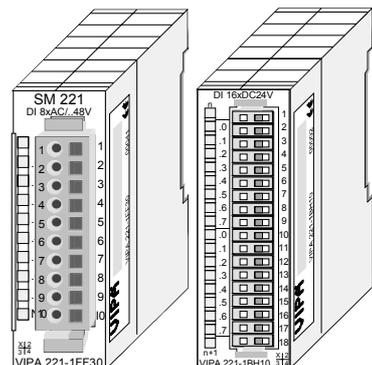
## Head modules



With a head module CPU respectively bus interface and DC 24V power supply are integrated to one casing.

Via the integrated power supply the CPU respectively bus interface is power supplied as well as the electronic of the connected periphery modules.

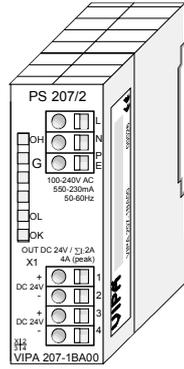
## Periphery modules



The modules are direct installed on a 35mm profile rail and connected to the head module by a bus connector, which was mounted on the profile rail before.

Most of the periphery modules are equipped with a 10pin respectively 18pin connector. This connector provides the electrical interface for the signaling and supplies lines of the modules.

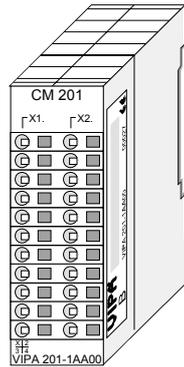
**Power supplies**



With the System 200V the DC 24V power supply can take place either externally or via a particularly for this developed power supply.

The power supply may be mounted on the profile rail together with the System 200V modules. It has no connector to the backplane bus.

**Expansion modules**



The expansion modules are complementary modules providing 2- or 3wire connection facilities.

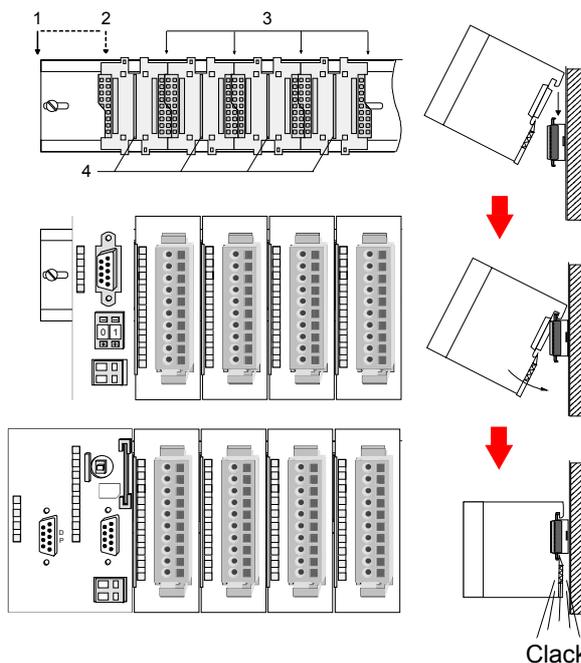
The modules are not connected to the backplane bus.

**Structure/ dimensions**

- Profile rail 35mm
- Dimensions of the basic enclosure:
  - 1tier width: (HxWxD) in mm: 76x25.4x74 in inches: 3x1x3
  - 2tier width: (HxWxD) in mm: 76x50.8x74 in inches: 3x2x3

**Installation**

Please note that you can only install head modules, like the CPU, the PC and couplers at slot 1 or 1 and 2 (for double width modules).



[1]	Head module (double width)
[2]	Head module (single width)
[3]	Periphery module
[4]	Guide rails

**Note**

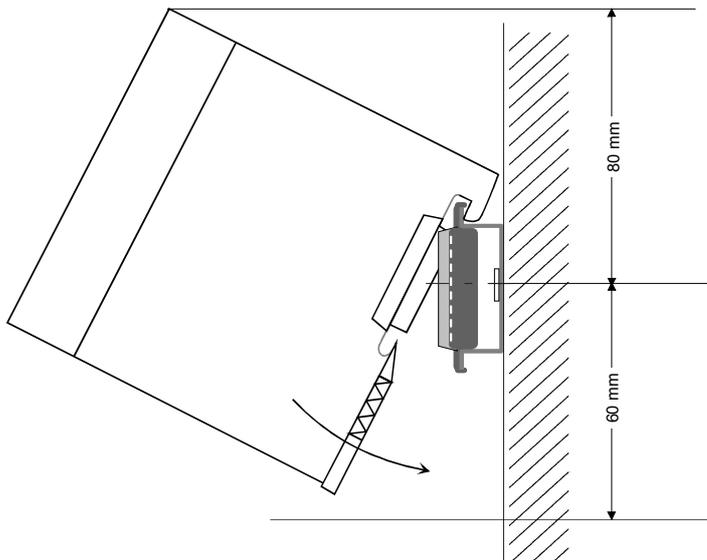
Information about the max. number of pluggable modules and the max. current at the backplane bus can be found in the "Technical Data" of the according head module.

Please install modules with a high current consumption directly beside the head module.

## Dimensions

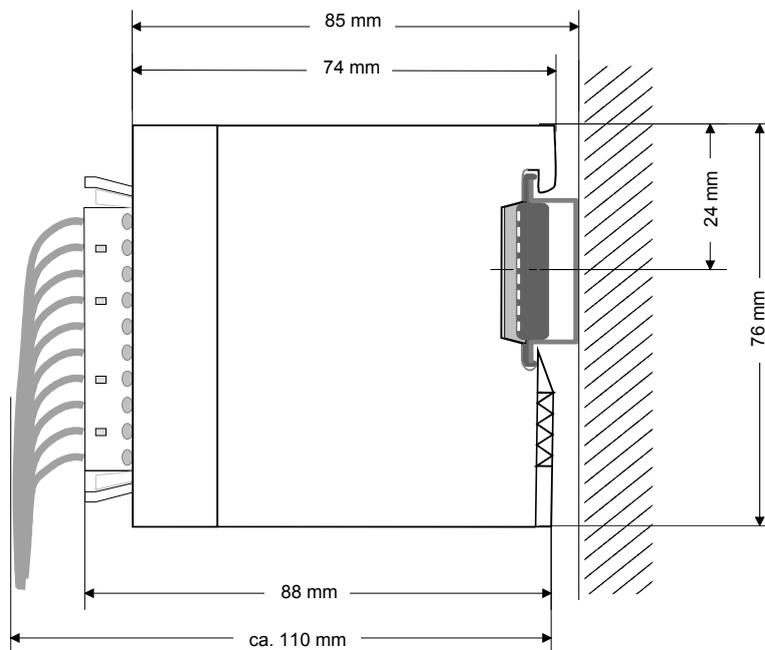
**Dimensions** 1tier width (HxWxD) in mm: 76 x 25.4 x 74  
**Basic enclosure** 2tier width (HxWxD) in mm: 76 x 50.8 x 74

### Installation dimensions

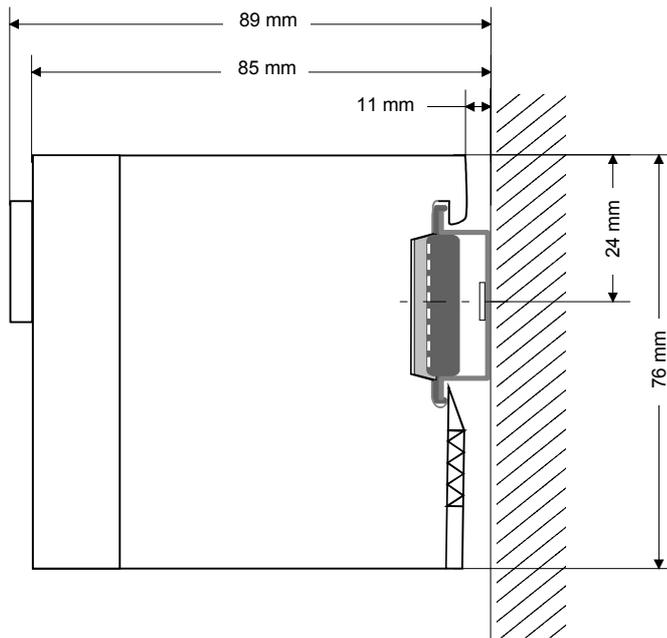


### Installed and wired dimensions

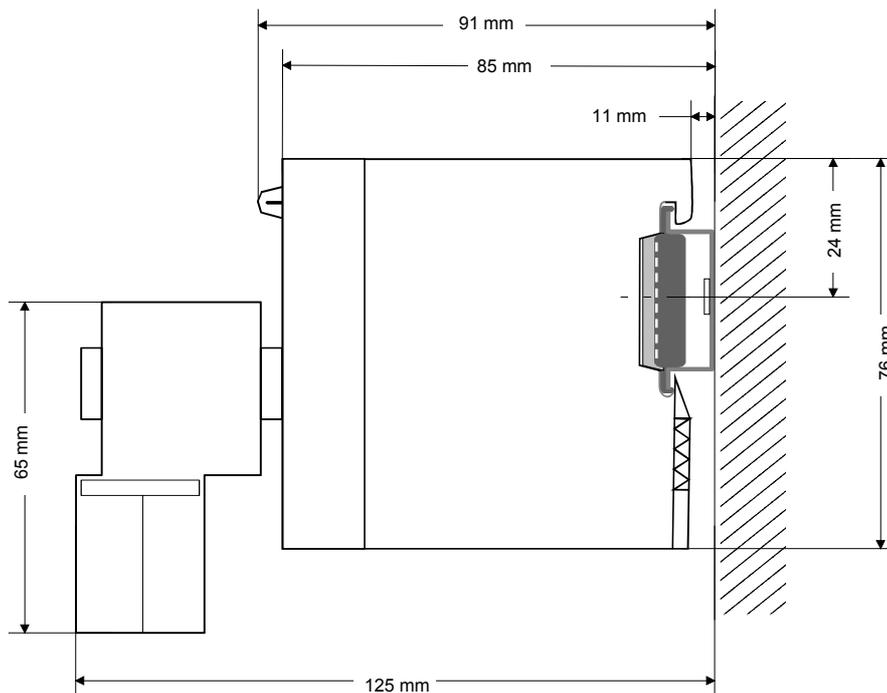
In- / Output modules



Function modules/  
Extension modules



CPUs (here with  
EasyConn from  
VIPA)



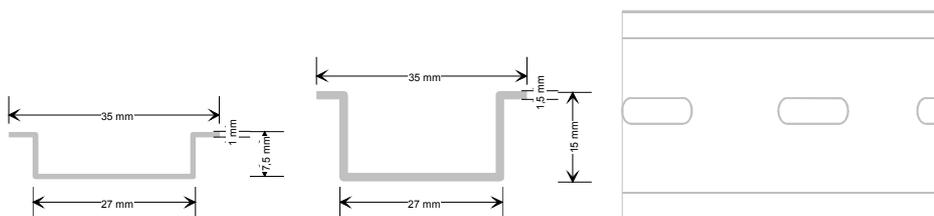
## Installation

### General

The modules are each installed on a 35mm profile rail and connected via a bus connector. Before installing the module the bus connector is to be placed on the profile rail before.

### Profile rail

For installation the following 35mm profile rails may be used:

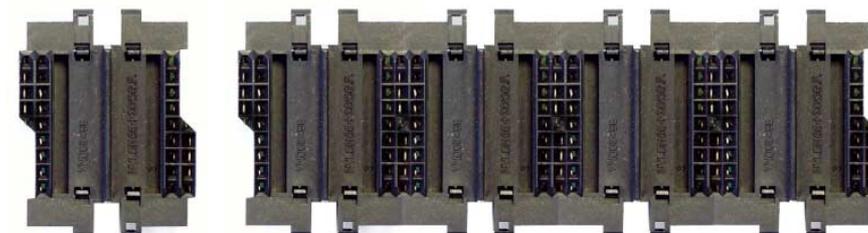


Order number	Label	Description
290-1AF00	35mm profile rail	Length 2000mm, height 15mm
290-1AF30	35mm profile rail	Length 530mm, height 15mm

### Bus connector

System 200V modules communicate via a backplane bus connector. The backplane bus connector is isolated and available from VIPA in of 1-, 2-, 4- or 8tier width.

The following figure shows a 1tier connector and a 4tier connector bus:



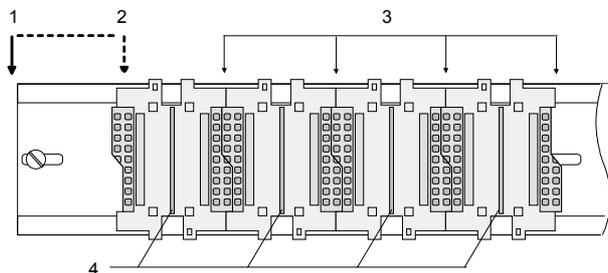
The bus connector is to be placed on the profile rail until it clips in its place and the bus connections look out from the profile rail.

Order number	Label	Description
290-0AA10	Bus connector	1tier
290-0AA20	Bus connector	2tier
290-0AA40	Bus connector	4tier
290-0AA80	Bus connector	8tier

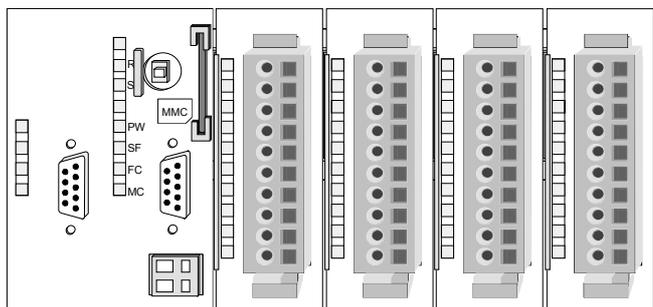
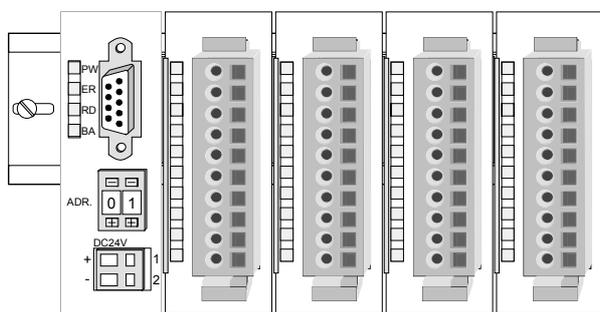
**Installation on a profile rail**

The following figure shows the installation of a 4tier width bus connector in a profile rail and the slots for the modules.

The different slots are defined by guide rails.



- [1] Head module (double width)
- [2] Head module (single width)
- [3] Peripheral module
- [4] Guide rails

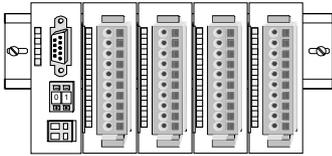


**Assembly regarding the current consumption**

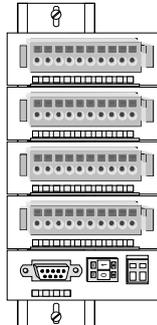
- Use bus connectors as long as possible.
- Sort the modules with a high current consumption right beside the head module. In the service area of [www.vipa.com](http://www.vipa.com) a list of current consumption of every System 200V module can be found.

**Assembly possibilities**

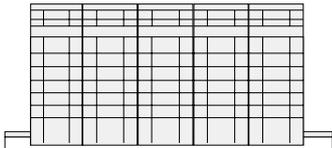
horizontal assembly



vertical assembly



lying assembly

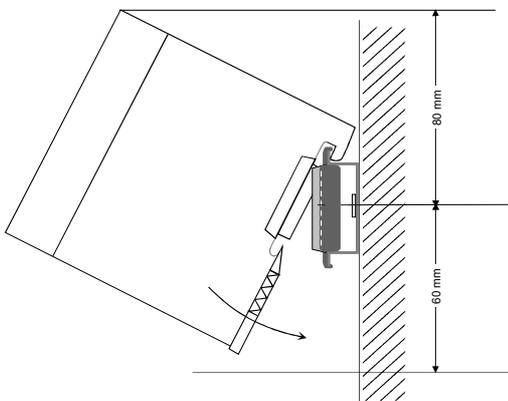


Please regard the allowed environmental temperatures:

- horizontal assembly: from 0 to 60°C
- vertical assembly: from 0 to 40°C
- lying assembly: from 0 to 40°C

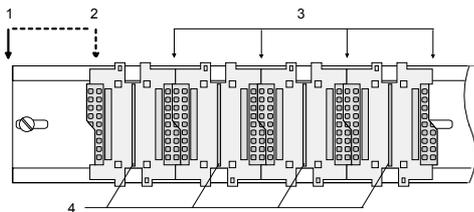
The horizontal assembly always starts at the left side with a head module, then you install the peripheral modules beside to the right.

You may install up to 32 peripheral modules.



**Please follow these rules during the assembly!**

- Turn off the power supply before you install or remove any modules!
- Make sure that a clearance of at least 60mm exists above and 80mm below the middle of the profile rail.



- Every row must be completed from left to right and it has to start with a head module.

- [1] Head module (double width)
- [2] Head module (single width)
- [3] Peripheral modules
- [4] Guide rails

- Modules are to be installed side by side. Gaps are not permitted between the modules since this would interrupt the backplane bus.
- A module is only installed properly and connected electrically when it has clicked into place with an audible click.
- Slots after the last module may remain unoccupied.

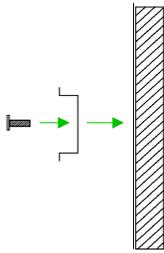


**Note!**

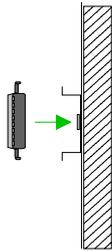
Information about the max. number of pluggable modules and the max. current at the backplane bus can be found in the "Technical Data" of the according head module.

Please install modules with a high current consumption directly beside the head module.

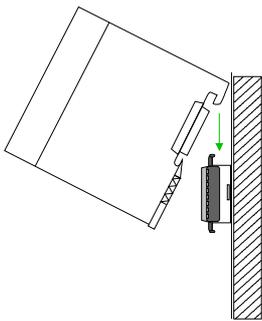
**Assembly procedure**



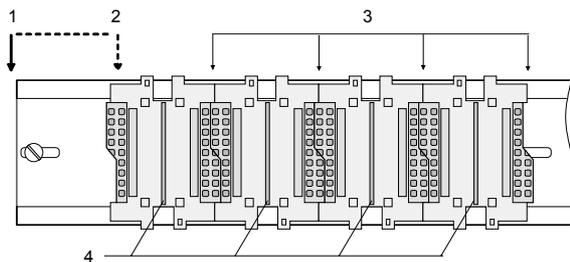
- Install the profile rail. Make sure that a clearance of at least 60mm exists above and 80mm below the middle of the profile rail.



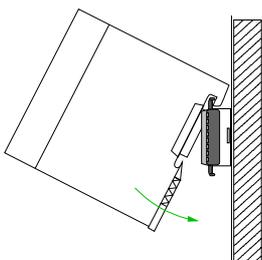
- Press the bus connector into the profile rail until it clips securely into place and the bus-connectors look out from the profile rail. This provides the basis for the installation of your modules.



- Start at the outer left location with the installation of your head module and install the peripheral modules to the right of this.



- [1] Head module (double width)
- [2] Head module (single width)
- [3] Peripheral module
- [4] Guide rails

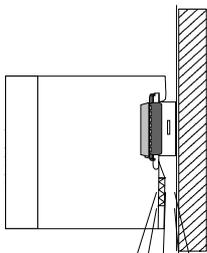


- Insert the module that you are installing into the profile rail at an angle of 45 degrees from the top and rotate the module into place until it clicks into the profile rail with an audible click. The proper connection to the backplane bus can only be guaranteed when the module has properly clicked into place.



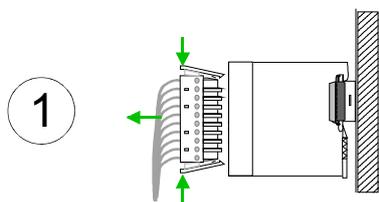
**Attention!**

Power must be turned off before modules are installed or removed!

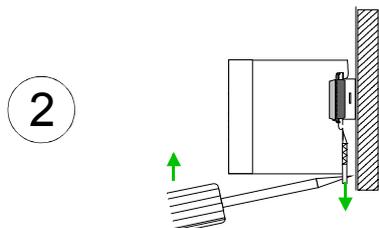


Clack

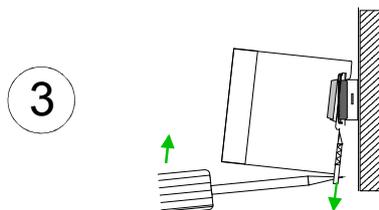
## Demounting and module exchange



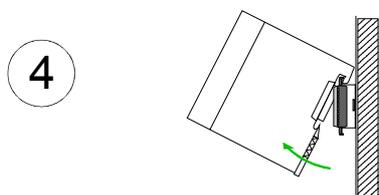
- Remove if exists the wiring to the module, by pressing both locking lever on the connector and pulling the connector.



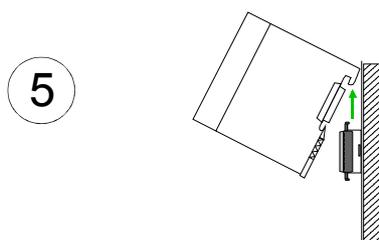
- The casing of the module has a spring loaded clip at the bottom by which the module can be removed.



- The clip is unlocked by pressing the screwdriver in an upward direction.



- Withdraw the module with a slight rotation to the top.



### Attention!

Power must be turned off before modules are installed or removed!

Please regard that the backplane bus is interrupted at the point where the module was removed!

## Wiring

### Overview

Most peripheral modules are equipped with a 10pole or a 18pole connector. This connector provides the electrical interface for the signaling and supply lines of the modules.

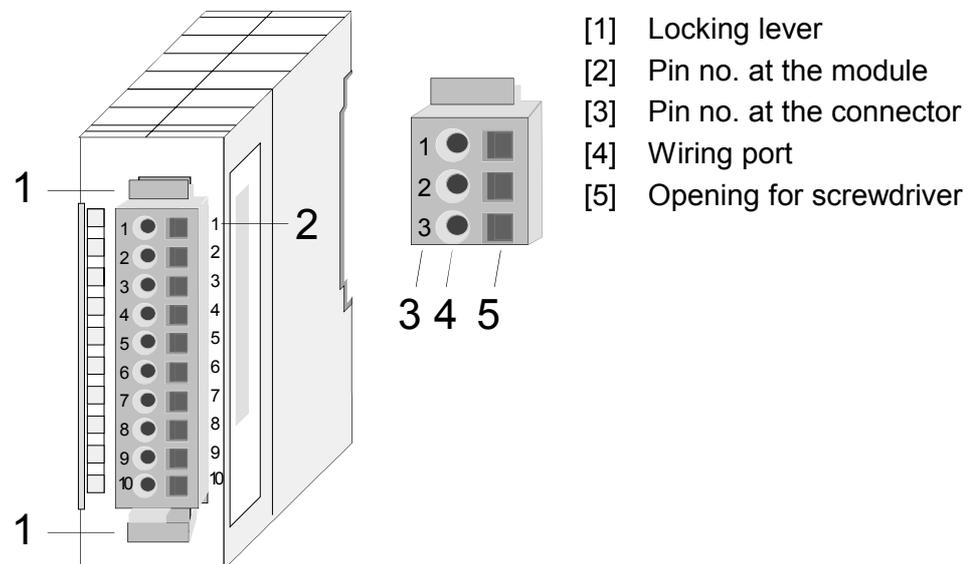
The modules carry spring-clip connectors for interconnections and wiring.

The spring-clip connector technology simplifies the wiring requirements for signaling and power cables.

In contrast to screw terminal connections, spring-clip wiring is vibration proof. The assignment of the terminals is contained in the description of the respective modules.

You may connect conductors with a diameter from 0.08mm<sup>2</sup> up to 2.5mm<sup>2</sup> (max. 1.5mm<sup>2</sup> for 18pole connectors).

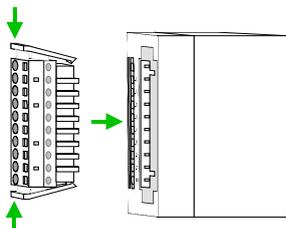
The following figure shows a module with a 10pole connector.



### Note!

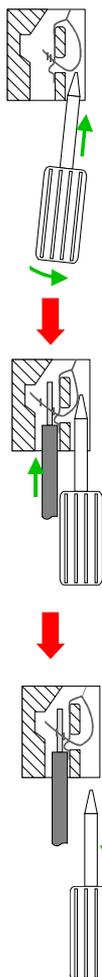
The spring-clip is destroyed if you push the screwdriver into the wire port! Make sure that you only insert the screwdriver into the square hole of the connector!

### Wiring procedure



- Install the connector on the module until it locks with an audible click. For this purpose you press the two clips together as shown. The connector is now in a permanent position and can easily be wired.

The following section shows the wiring procedure from top view.



- Insert a screwdriver at an angle into the square opening as shown.
- Press and hold the screwdriver in the opposite direction to open the contact spring.

- Insert the stripped end of the wire into the round opening. You can use wires with a diameter of 0.08mm<sup>2</sup> to 2.5mm<sup>2</sup> (1.5mm<sup>2</sup> for 18pole connectors).

- By removing the screwdriver the wire is connected safely with the plug connector via a spring.



#### Note!

Wire the power supply connections first followed by the signal cables (inputs and outputs).

## Installation guidelines

**General** The installation guidelines contain information about the interference free deployment of System 200V systems. There is the description of the ways, interference may occur in your control, how you can make sure the electromagnetic digestibility (EMC), and how you manage the isolation.

**What means EMC?** Electromagnetic digestibility (EMC) means the ability of an electrical device, to function error free in an electromagnetic environment without being interferenced res. without interfering the environment.  
All System 200V components are developed for the deployment in hard industrial environments and fulfill high demands on the EMC. Nevertheless you should project an EMC planning before installing the components and take conceivable interference causes into account.

**Possible interference causes** Electromagnetic interferences may interfere your control via different ways:

- Fields
- I/O signal conductors
- Bus system
- Current supply
- Protected earth conductor

Depending on the spreading medium (lead bound or lead free) and the distance to the interference cause, interferences to your control occur by means of different coupling mechanisms.

One differs:

- galvanic coupling
- capacitive coupling
- inductive coupling
- radiant coupling

**Basic rules for EMC**

In the most times it is enough to take care of some elementary rules to guarantee the EMC. Please regard the following basic rules when installing your PLC.

- Take care of a correct area-wide grounding of the inactive metal parts when installing your components.
  - Install a central connection between the ground and the protected earth conductor system.
  - Connect all inactive metal extensive and impedance-low.
  - Please try not to use aluminum parts. Aluminum is easily oxidizing and is therefore less suitable for grounding.
- When cabling, take care of the correct line routing.
  - Organize your cabling in line groups (high voltage, current supply, signal and data lines).
  - Always lay your high voltage lines and signal res. data lines in separate channels or bundles.
  - Route the signal and data lines as near as possible beside ground areas (e.g. suspension bars, metal rails, tin cabinet).
- Proof the correct fixing of the lead isolation.
  - Data lines must be laid isolated.
  - Analog lines must be laid isolated. When transmitting signals with small amplitudes the one sided laying of the isolation may be favorable.
  - Lay the line isolation extensively on an isolation/protected earth conductor rail directly after the cabinet entry and fix the isolation with cable clamps.
  - Make sure that the isolation/protected earth conductor rail is connected impedance-low with the cabinet.
  - Use metallic or metalized plug cases for isolated data lines.
- In special use cases you should appoint special EMC actions.
  - Wire all inductivities with erase links.
  - Please consider luminescent lamps can influence signal lines.
- Create a homogeneous reference potential and ground all electrical operating supplies when possible.
  - Please take care for the targeted employment of the grounding actions. The grounding of the PLC is a protection and functionality activity.
  - Connect installation parts and cabinets with the System 200V in star topology with the isolation/protected earth conductor system. So you avoid ground loops.
  - If potential differences between installation parts and cabinets occur, lay sufficiently dimensioned potential compensation lines.

**Isolation of conductors**

Electrical, magnetically and electromagnetic interference fields are weakened by means of an isolation, one talks of absorption.

Via the isolation rail, that is connected conductive with the rack, interference currents are shunt via cable isolation to the ground. Hereby you have to make sure, that the connection to the protected earth conductor is impedance-low, because otherwise the interference currents may appear as interference cause.

When isolating cables you have to regard the following:

- If possible, use only cables with isolation tangle.
- The hiding power of the isolation should be higher than 80%.
- Normally you should always lay the isolation of cables on both sides. Only by means of the both-sided connection of the isolation you achieve high quality interference suppression in the higher frequency area.  
Only as exception you may also lay the isolation one-sided. Then you only achieve the absorption of the lower frequencies. A one-sided isolation connection may be convenient, if:
  - the conduction of a potential compensating line is not possible
  - analog signals (some mV res.  $\mu$ A) are transferred
  - foil isolations (static isolations) are used.
- With data lines always use metallic or metalized plugs for serial couplings. Fix the isolation of the data line at the plug rack. Do not lay the isolation on the PIN 1 of the plug bar!
- At stationary operation it is convenient to strip the insulated cable interruption free and lay it on the isolation/protected earth conductor line.
- To fix the isolation tangles use cable clamps out of metal. The clamps must clasp the isolation extensively and have well contact.
- Lay the isolation on an isolation rail directly after the entry of the cable in the cabinet. Lead the isolation further on to the System 200V module and **don't** lay it on there again!

**Please regard at installation!**

At potential differences between the grounding points, there may be a compensation current via the isolation connected at both sides.

Remedy: Potential compensation line.

## General data

### Structure/ dimensions

- Profile rail 35mm
- Peripheral modules with recessed labelling
- Dimensions of the basic enclosure:  
1tier width: (HxWxD) in mm: 76x25.4x74 in inches: 3x1x3  
2tier width: (HxWxD) in mm: 76x50.8x74 in inches: 3x2x3

### Reliability

- Wiring by means of spring pressure connections (CageClamps) at the front-facing connector, core cross-section 0.08 ... 2.5mm<sup>2</sup> or 1.5mm<sup>2</sup> (18pole plug)
- Complete isolation of the wiring when modules are exchanged
- Every module is isolated from the backplane bus
- ESD/Burst acc. IEC 61000-4-2 / IEC 61000-4-4 (to level 3)
- Shock resistance acc. IEC 60068-2-6 / IEC 60068-2-27 (1G/12G)
- Class of protection IP20

### Environmental conditions

- Operating temperature: 0 ... +60°C
- Storage temperature: -25 ... +70°C
- Relative humidity: 5 ... 95% without condensation
- Ventilation by means of a fan is not required



## Chapter 2 Hardware description

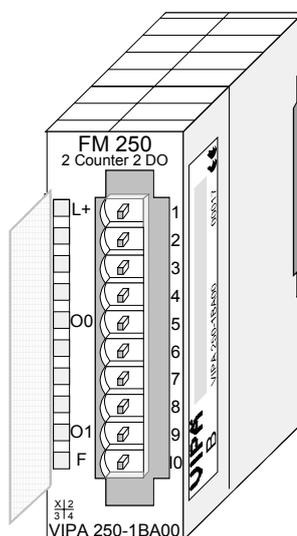
**Overview** Here the hardware components of the FM 250-1BA00 are described.  
The technical data are at the end of the chapter.

<b>Contents</b>	<b>Topic</b>	<b>Page</b>
	<b>Chapter 2 Hardware description.....</b>	<b>2-1</b>
	Properties.....	2-2
	Structure .....	2-3
	Technical data.....	2-4

## Properties

### FM 250 250-1BA00

- 2 channels with each 32Bit /  
4 channels with each 16Bit (depending on the mode)
- DC 24V supply voltage via front and via backplane bus
- free configurable DC 24V outputs (max. 1A)
- Counter and compare registers are loaded by means of a control byte
- Standard up-down counter with a resolution of 32Bit or 16Bit
- Compare and auto-reload functions
- Different modes for encoder pulses
- Pulse-width measurements and frequency measurements



#### Note!

The following information is only applicable to counter modules with order no.: VIPA 250-1BA00 and a revision level 5 and higher.

#### Order data

Type	Order number	Description
FM 250	VIPA 250-1BA00	Counter module (2 counter 2 DO)

## Structure

### Functionality

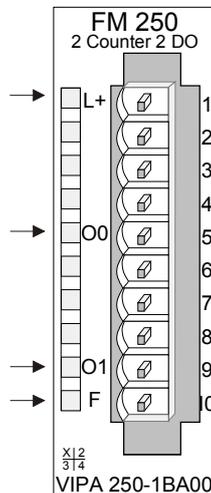
The counter module accepts the signals from transducers connected to the module and processes these pulses in accordance with the selected mode of operation. The module has 2/4 channels with a data resolution of 32/16Bit each.

These modules provide 40 counter modes and two 24V outputs they are controlled in accordance with the selected mode.

### Status indicator pin assignment

**LED Description**

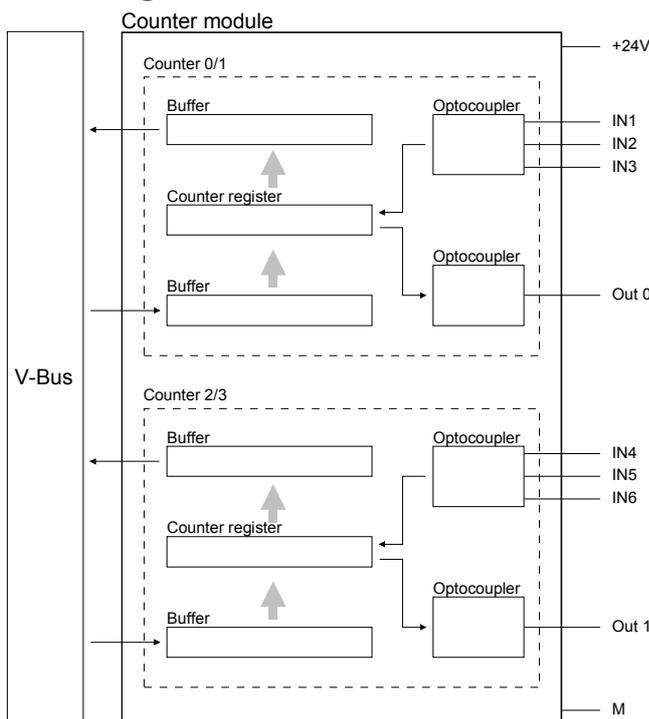
- L+ LED (green)  
Supply voltage available
- O0 LED (green)  
Output counter 0
- O1 LED (green)  
Output counter 1
- F LED (red)  
Error /overload



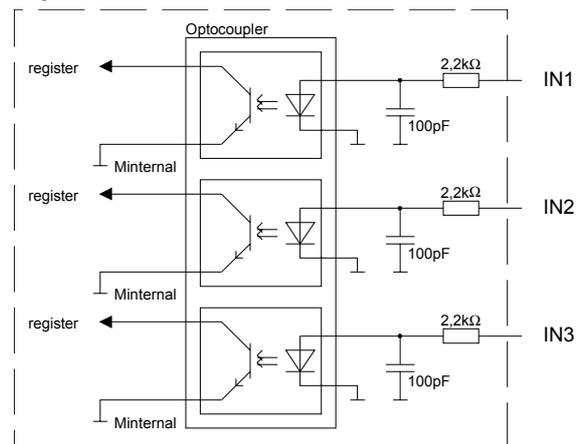
**Pin Assignment**

- 1 Supply voltage +24V DC
- 2 IN1 input 1 counter 0/1
- 3 IN2 input 2 counter 0/1
- 4 IN3 input 3 counter 0/1
- 5 OUT0 output counter 0/1
- 6 IN4 input 4 counter 2/3
- 7 IN5 input 5 counter 2/3
- 8 IN6 input 6 counter 2/3
- 9 OUT1 output counter 2/3
- 10 Common of supply voltage

### Block diagram



### Input internal circuit



## Technical data

<b>Order number</b>	<b>250-1BA00</b>
Type	FM 250
<b>Current consumption/power loss</b>	
Current consumption from backplane bus	80 mA
Power loss	2.5 W
<b>Technical data digital inputs</b>	
Number of inputs	6
Cable length, shielded	1000 m
Cable length, unshielded	600 m
Rated load voltage	DC 24 V
Reverse polarity protection of rated load voltage	✓
Current consumption from load voltage L+ (without load)	-
Rated value	-
Input voltage for signal "0"	DC 0...5 V
Input voltage for signal "1"	DC 15...28.8 V
Input voltage hysteresis	-
Frequency range	-
Input resistance	2 kΩ
Input current for signal "1"	14 mA
Connection of Two-Wire-BEROs possible	-
Max. permissible BERO quiescent current	-
Input delay of "0" to "1"	0,8 μs
Input delay of "1" to "0"	0,8 μs
Number of simultaneously utilizable inputs horizontal configuration	6
Number of simultaneously utilizable inputs vertical configuration	6
Input characteristic curve	-
Initial data size	10 Byte
<b>Technical data digital outputs</b>	
Number of outputs	2
Cable length, shielded	1000 m
Cable length, unshielded	600 m
Rated load voltage	DC 24 V
Reverse polarity protection of rated load voltage	✓
Current consumption from load voltage L+ (without load)	10 mA
Total current per group, horizontal configuration, 40°C	-
Total current per group, horizontal configuration, 60°C	-
Total current per group, vertical configuration	-
Output voltage signal "1" at min. current	L+ (-0.8 V)
Output voltage signal "1" at max. current	-
Output current at signal "1", rated value	2 A
Output current, permitted range to 40°C	-
Output current, permitted range to 60°C	-
Output current at signal "0" max. (residual current)	-
Output delay of "0" to "1"	max. 100 μs
Output delay of "1" to "0"	max. 500 μs
Minimum load current	-
Lamp load	10 W
Parallel switching of outputs for redundant control of a load	-
Parallel switching of outputs for increased power	-
Actuation of digital input	-
Switching frequency with resistive load	max. 1000 Hz

<b>Order number</b>	<b>250-1BA00</b>
Switching frequency with inductive load	max. 0.5 Hz
Switching frequency on lamp load	max. 10 Hz
Internal limitation of inductive shut-off voltage	L+ (-52 V)
Short-circuit protection of output	yes, electronic
Trigger level	3 A
Number of operating cycle of relay outputs	-
Switching capacity of contacts	-
Output data size	10 Byte
<b>Technical data counters</b>	
Number of counters	2
Counter width	1x32 Bit / 2x16 Bit
Maximum input frequency	1 MHz
Maximum count frequency	1 MHz
Mode incremental encoder	✓
Mode pulse / direction	✓
Mode pulse	✓
Mode frequency counter	✓
Mode period measurement	✓
Gate input available	✓
Latch input available	-
Reset input available	✓
Counter output available	✓
<b>Status information, alarms, diagnostics</b>	
Status display	yes
Interrupts	no
Process alarm	no
Diagnostic interrupt	no
Diagnostic functions	no
Diagnostics information read-out	none
Supply voltage display	yes
Group error display	red LED
Channel error display	none
<b>Isolation</b>	
Between channels	-
Between channels of groups to	-
Between channels and backplane bus	✓
Between channels and power supply	-
Max. potential difference between circuits	-
Max. potential difference between inputs (Ucm)	-
Max. potential difference between Mana and Mintern (Uiso)	-
Max. potential difference between inputs and Mana (Ucm)	-
Max. potential difference between inputs and Mintern (Uiso)	-
Max. potential difference between Mintern and outputs	-
Insulation tested with	DC 500 V
<b>Datasizes</b>	
Input bytes	10
Output bytes	10
Parameter bytes	4
Diagnostic bytes	0
<b>Housing</b>	
Material	PPE / PA 6.6
Mounting	Profile rail 35 mm
<b>Mechanical data</b>	
Dimensions (WxHxD)	25.4 x 76 x 78 mm

<b>Order number</b>	<b>250-1BA00</b>
Weight	230 g
<b>Environmental conditions</b>	
Operating temperature	0 °C to 60 °C
Storage temperature	-25 °C to 70 °C
<b>Certifications</b>	
UL508 certification	yes

## Chapter 3 Deployment

**Overview** This chapter provides information to the configuration and the various counter modes of the Counter module FM 250 are described.

<b>Contents</b>	<b>Topic</b>	<b>Page</b>
	<b>Chapter 3 Deployment .....</b>	<b>3-1</b>
	Data input / output.....	3-2
	Summary of counter modes and interfacing .....	3-3
	Counter modes.....	3-6

## Data input / output

### Access to the counter module

The module has 2/4 channels with a resolution of 32/16Bit each. You may use parameters to specify the mode for each channel res. channel pair. The pin assignment for the channel depends upon the selected mode (see description of modes).

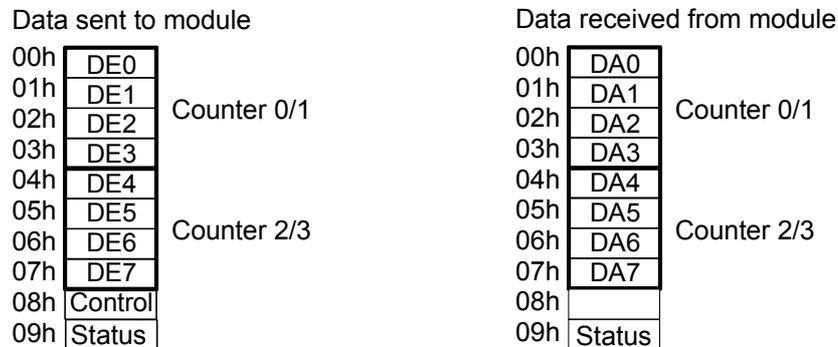
10 data bytes are required for the data input and output. Data output to a counter channel requires 10Byte, for example for defaults or for comparison values. In the latter case Byte 9 (control) is used to initiate a write operation into the required counter register. The respective values are transferred into the counter registers when they are toggled (0 → 1).

The 10. byte (status byte) controls the behavior of the counter during a restart of the next higher master module. You may set the counter level to retentive by means of a combination of Bits 0 and 1; i.e. the original counter level will not be reset when the next higher master module restarts.

The following combinations are possible:

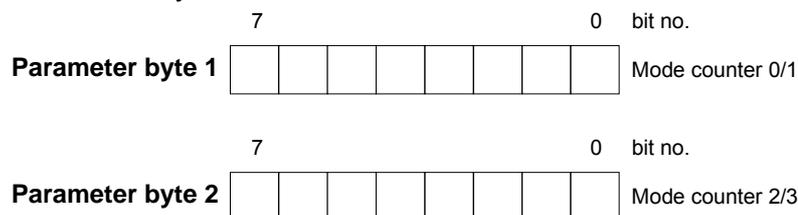
- Bit 0 = 1, Bit 1 = 0      counter value is retentive during restart
- Bit 0 = x, Bit 1 = 1      counter value is reset during restart (default)

You may check your settings at any time by reading Byte 10 of the output data.



### Configuration parameters

The configuration parameters consist of 2Byte. You use these bytes to define the operating mode of each channel by means of a mode number. This chapter contains a detailed description of the different modes further below. The different combinations of the various modes are available from the table on the next page. The procedure for the transfer of parameter bytes is available from the description for the System 200V bus coupler or the master system.



## Summary of counter modes and interfacing

Mode	may be combined	Function	IN1	IN2	IN3	IN4	IN5	IN6	OUT0	OUT1	Auto Re-load	Compare Load
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
0	yes	32bit counter	RES	CLK	DIR	RST	CLK	DIR	=0	=0	no	=0
1	yes	Encoder 1 edge	RES	A	B	RST	A	B	=0	=0	no	=0
3	yes	Encoder 2 edges	RES	A	B	RST	A	B	=0	=0	no	=0
5	yes	Encoder 4 edges	RES	A	B	RST	A	B	=0	=0	no	=0
			<b>Counter 1 counter 0</b>			<b>Counter 3 counter 2</b>						
8	yes	2x16bit counter up/up	-	CLK	CLK	-	CLK	CLK	-	-	no	no
9	yes	2x16bit counter down/up	-	CLK	CLK	-	CLK	CLK	-	-	no	no
10	yes	2x16bit counter up/down	-	CLK	CLK	-	CLK	CLK	-	-	no	no
11	yes	2x16bit counter down/down	-	CLK	CLK	-	CLK	CLK	-	-	no	no
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
12	yes	32bit counter up + gate	RES	CLK	Gate	RST	CLK	Gate	=comp	=comp	no	yes
13	yes	32bit counter down + gate	RES	CLK	Gate	RST	CLK	Gate	=comp	=comp	no	yes
14	yes	32bit counter up + gate	RES	CLK	Gate	RST	CLK	Gate	=comp	=comp	yes	yes
15	yes	32bit counter down + gate	RES	CLK	Gate	RST	CLK	Gate	=comp	=comp	yes	yes
			<b>Combination of counter 0 ... 3</b>									
16	no	Frequency measurement	RES	CLK	Start	Stop	-	-	Meas. active	Meas. compl.	no	yes
17	no	Period measurement	RES	CLK	Start	Stop	-	-	Meas. active	Meas. compl.	no	yes
18	no	Frequency measurement with gate output	RES	CLK	Start	Stop	-	-	Meas. gate	Meas. gate	no	yes
19	no	Period measurement with gate output	RES	CLK	Start	Stop	-	-	Meas. gate	Meas. gate	no	yes
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
6	yes	Pulse low, 50kHz with Direction Input	RES	Pulse	DIR	RES	Pulse	DIR	-	-		
20	yes	Pulse low, prog. time base with Direction Input	RES	Pulse	DIR	RES	Pulse	DIR	-	-		
21	yes	Pulse low, up, prog. time base with Gate	RES	Pulse	Gate	RES	Pulse	Gate	-	-		
22	yes	Pulse high, up, prog. time base with Gate	RES	Pulse	Gate	RES	Pulse	Gate	-	-		
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
23	yes	One Shot, up, Set	RES	CLK	Gate	RES	CLK	Gate	1 if active	1 if active	no	yes
24	yes	One Shot, down, Set	RES	CLK	Gate	RES	CLK	Gate	1 if active	1 if active	no	yes
25	yes	One Shot, up, Reset	RES	CLK	Gate	RES	CLK	Gate	0 if active	0 if active	no	yes
26	yes	One Shot, down, Reset	RES	CLK	Gate	RES	CLK	Gate	0 if active	0 if active	no	yes
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
27	yes	32 bit counter	Gate/R <sup>†</sup>	CLK	DIR	Gate/R <sup>†</sup>	CLK	DIR	=0	=0	no	=0
28	yes	Encoder 1 edge	Gate/R <sup>†</sup>	A	B	Gate/R <sup>†</sup>	A	B	=0	=0	no	=0
29	yes	Encoder 2 edges	Gate/R <sup>†</sup>	A	B	Gate/R <sup>†</sup>	A	B	=0	=0	no	=0
30	yes	Encoder 4 edges	Gate/R <sup>†</sup>	A	B	Gate/R <sup>†</sup>	A	B	=0	=0	no	=0

continued ...

... continue

Mode	may be combined	Function	IN1	IN2	IN3	IN4	IN5	IN6	OUT0	OUT1	Auto Re-load	Compare Load
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
31	yes	32Bit counter up+Gate	RES <sup>†</sup>	CLK	Gate	RES <sup>†</sup>	CLK	Gate	=comp	=comp	no	yes
32	yes	32Bit counter down+Gate	RES <sup>†</sup>	CLK	Gate	RES <sup>†</sup>	CLK	Gate	=comp	=comp	no	yes
33	yes	32Bit counter up+Gate	RES <sup>†</sup>	CLK	Gate	RES <sup>†</sup>	CLK	Gate	=comp	=comp	yes	yes
34	yes	32Bit counter down+Gate	RES <sup>†</sup>	CLK	Gate	RES <sup>†</sup>	CLK	Gate	=comp	=comp	yes	yes
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
35	yes	32Bit counter	Gate	CLK	DIR	Gate	CLK	DIR	=0	=0	no	=0
36	yes	Encoder 1 edge	Gate	A	B	Gate	A	B	=0	=0	no	=0
37	yes	Encoder 2 edges	Gate	A	B	Gate	A	B	=0	=0	no	=0
38	yes	Encoder 4 edges	Gate	A	B	Gate	A	B	=0	=0	no	=0
			<b>Counter 0/1</b>			<b>Counter 2/3</b>						
39	yes	32Bit counter up+Gate	RES <sup>†</sup>	Gate		RES <sup>†</sup>	Gate		-	-	-	-
40	yes	32Bit counter down+Gate	RES <sup>†</sup>	Gate		RES <sup>†</sup>	Gate		-	-	-	-
41	yes	32Bit counter up+Gate	RES <sup>†</sup>	Gate		RES <sup>†</sup>	Gate		-	-	-	-
42	yes	32Bit counter down+Gate	RES <sup>†</sup>	Gate		RES <sup>†</sup>	Gate		-	-	-	-

Due to technical advances the revision level and the functionality of the counter module was continuously expanded. Below follows a list that allocates the different modes to the revision level:

Mode 0-5	revision level 3	Mode 27-30	revision level 8/9
Mode 0-17	revision level 4	Mode 31-38	revision level 10
Mode 0-19	revision level 5	Mode 39-42	revision level 11
Mode 6, 20-26	revision level 6/7		

**Terminology:**

**RES**                      RESET signal that has to be LOW during the measuring process. A HIGH level (level triggered) erases one or both counters, depending on the selected mode.

**RES<sup>†</sup>**                    The counter is reset by the rising edge of this signal (edge triggered).

**CLK**                      The clock signal from the connected transducer.

**Start or Stop**            A HIGH level starts or stops the counter. When the start level is active, the counter will start with the next CLK pulse that corresponds to the selected mode.

**DIR**                      In mode 0 the level of the DIR signal determines the direction of the counting process.  
 LOW level: count up  
 HIGH level: count down

**Auto Reload** The Auto Reload function transfers a user-defined value into the counter when the counter reaches the number contained in the compare register.

**Compare Load** You may use the compare function to specify an stop value for the counter. Depending on the selected mode an output is activated or the counter is re-started when it reaches this value.

**Gate** Gate signal enabling the counter.

**Gate/R<sup>↑</sup>** The counter is reset by the rising edge of this signal. As long as the signal is at "1", the counter is released.  
(Gate = level triggered; R<sup>↑</sup> = edge triggered)

**Measurement gate** Status indicator of the counter activity - is set to a HIGH level after the 1. CLK signal and LOW level after the last CLK signal (mode 18 ... 19).

**Pulse** The pulse width of the introduced signal is determined by means of the internal time base.

**Fref** Reference or clock frequency that is set permanently to 50kHz in mode 6. The clock frequency "Fref" for counter modes 20-22, 39-42 is programmable:

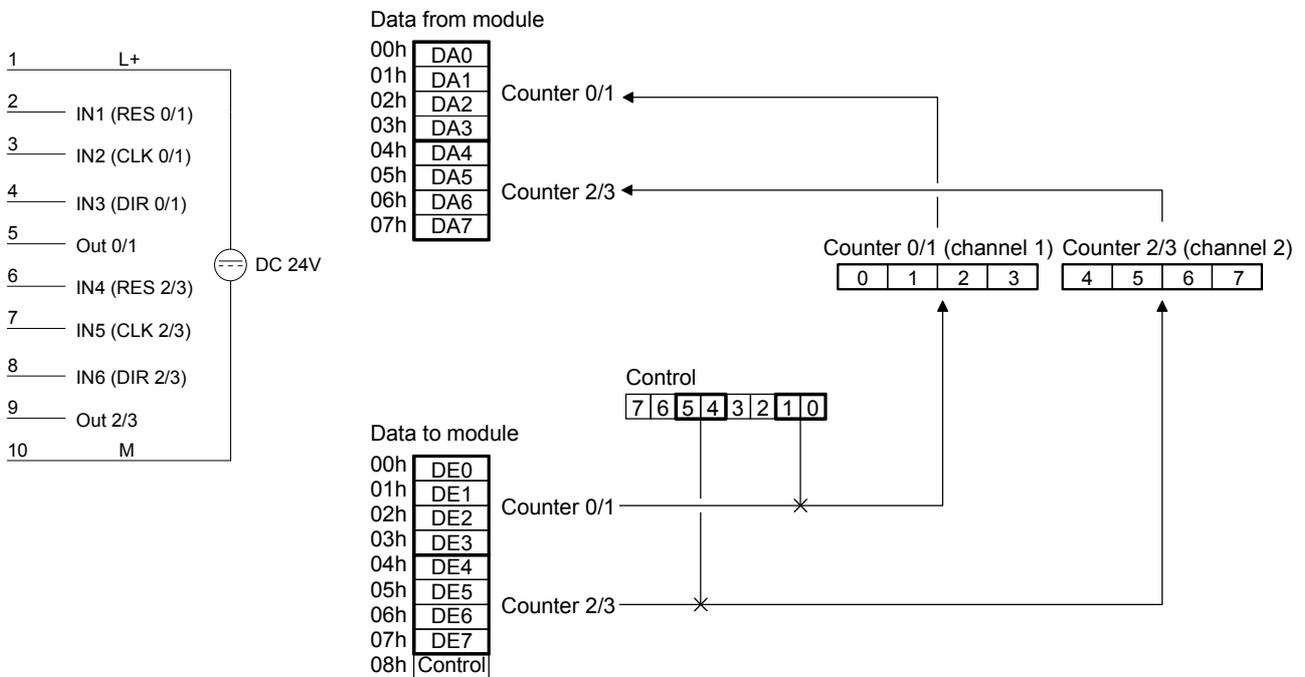
Parameter	Fref
0	10MHz
1	1MHz
2	100kHz
3	10kHz

# Counter modes

## Mode 0 32Bit counter

2x 32Bit Counter. You determine the direction by means of the DIR input (IN3 or IN6). Every rising or falling edge of the input clock signal increments or decrements the counter. During the counting process the RES signal must be at a LOW level. If the RES signal is at a HIGH level, the counter is cleared. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter should continue counting. If the counter stops at zero, the output remains active.

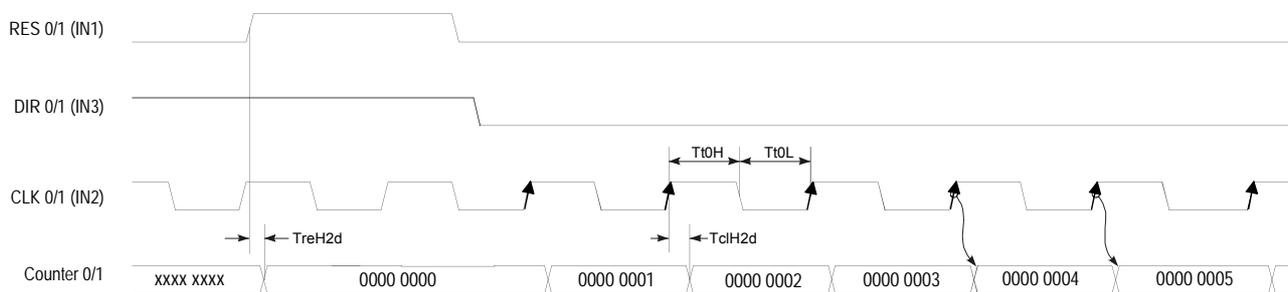
### Pin assignment access to counter



**Up counter**

In mode 0, a LOW level at the DIR input configures the counter for counting up.

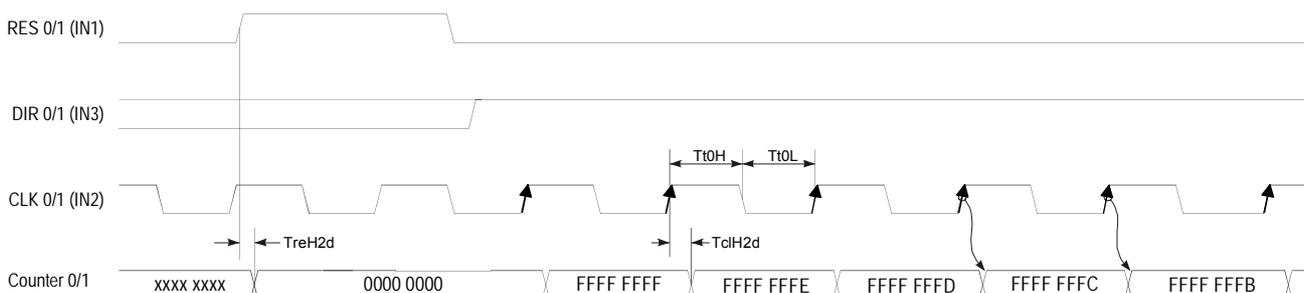
Timing diagram of the counter 0/1 example:



**Down counter**

In mode 0, a HIGH level at the DIR input configures the counter for counting down.

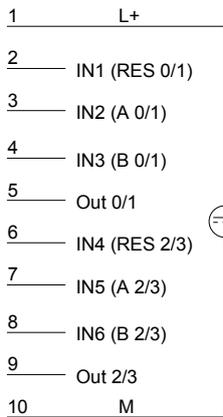
Timing diagram of the counter 0/1 example:



**Mode 1  
Encoder 1 edge**

In mode 1 you may configure an encoder for one of the channels. Depending on the direction of rotation this encoder will increment or decrement the internal counter with every falling edge. The RES input has to be at a LOW level during the counting process. A HIGH level clears the counter. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero the output remains active.

**Pin assignment  
access to counter**

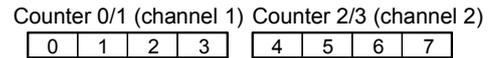


Data from module

00h	DA0
01h	DA1
02h	DA2
03h	DA3
04h	DA4
05h	DA5
06h	DA6
07h	DA7

Counter 0/1

Counter 2/3



Control

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Data to module

00h	DE0
01h	DE1
02h	DE2
03h	DE3
04h	DE4
05h	DE5
06h	DE6
07h	DE7
08h	Control

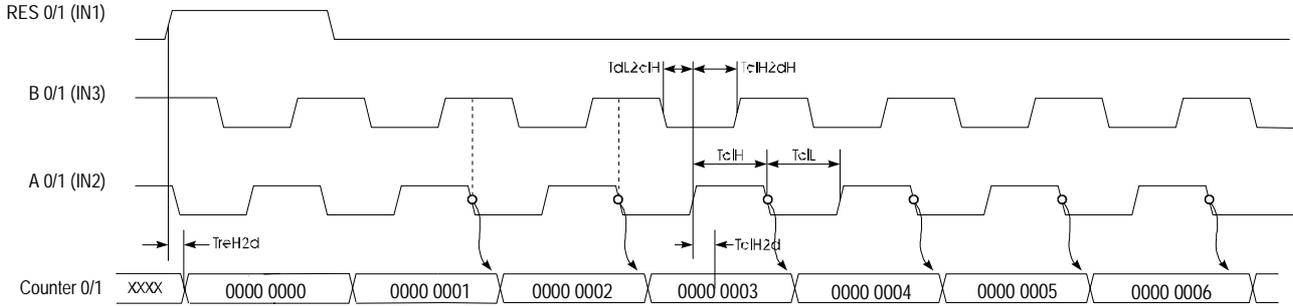
Counter 0/1

Counter 2/3

**Up counter**

Every falling edge of the signal at input A increments the counter if input B is at HIGH level at this moment.

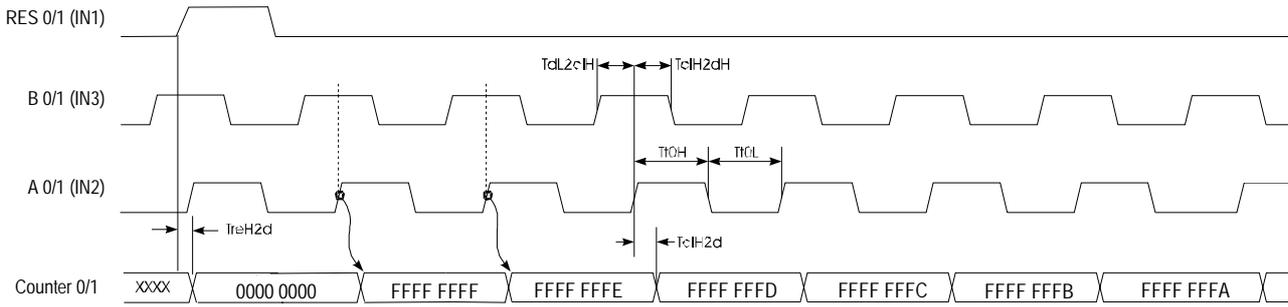
Timing diagram for the counter 0/1 example:



**Down counter**

Every rising edge of the signal at input A decrements the internal counter if input B is at HIGH level at this moment.

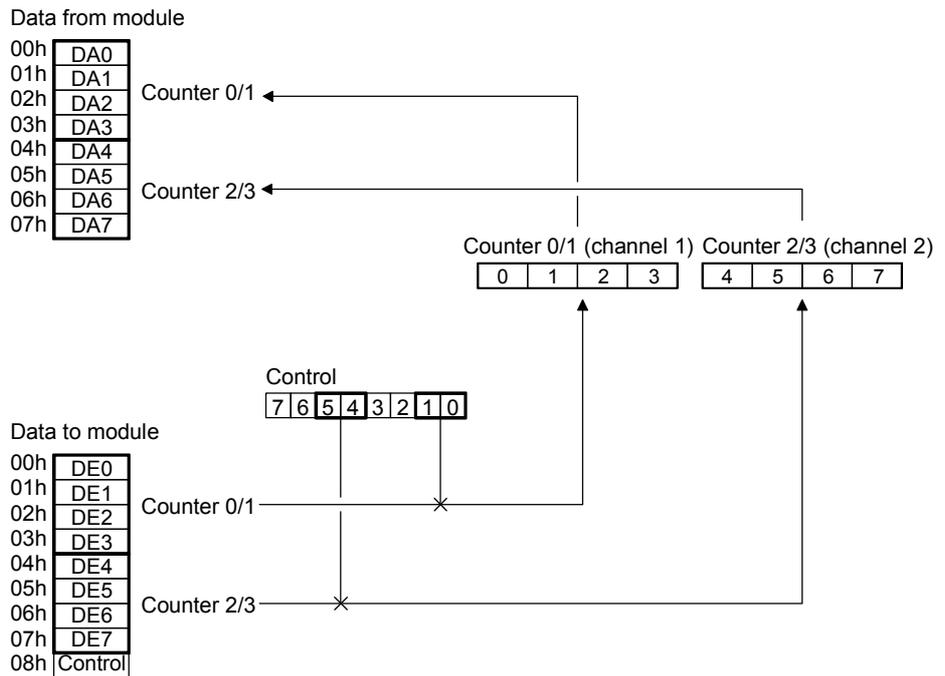
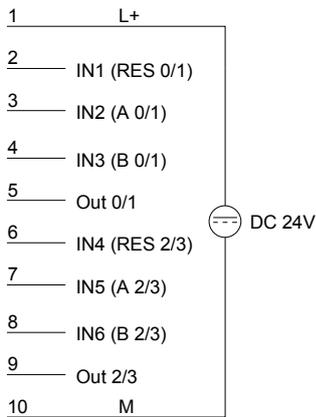
Timing diagram for the counter 0/1 example:



**Mode 3  
Encoder 2 edges**

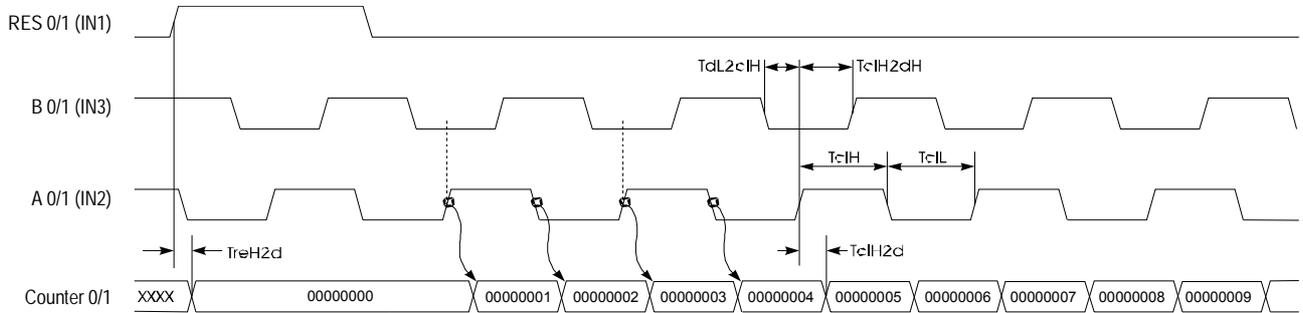
Every rising or falling edge of the signal at input A changes the counter by 1. The direction of the count depends on the level of the signal applied to input B. RES has to be at a LOW level during the counting process. A HIGH level clears the counter. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero the output remains active.

**Pin assignment  
access to counter**



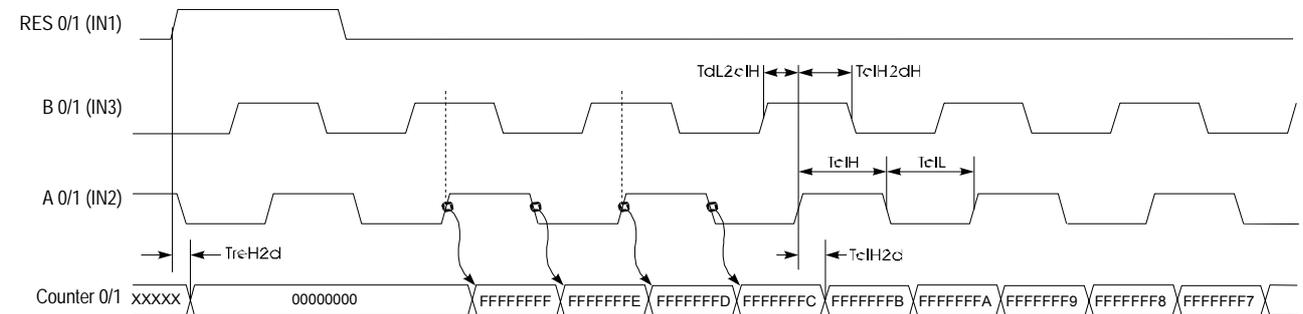
**Up counter**

The counter is incremented by the rising edge of signal A if input B is at a LOW level or by the falling edge of input A when input B is at a HIGH level. Timing diagram for the counter 0/1 example:



**Down-counter**

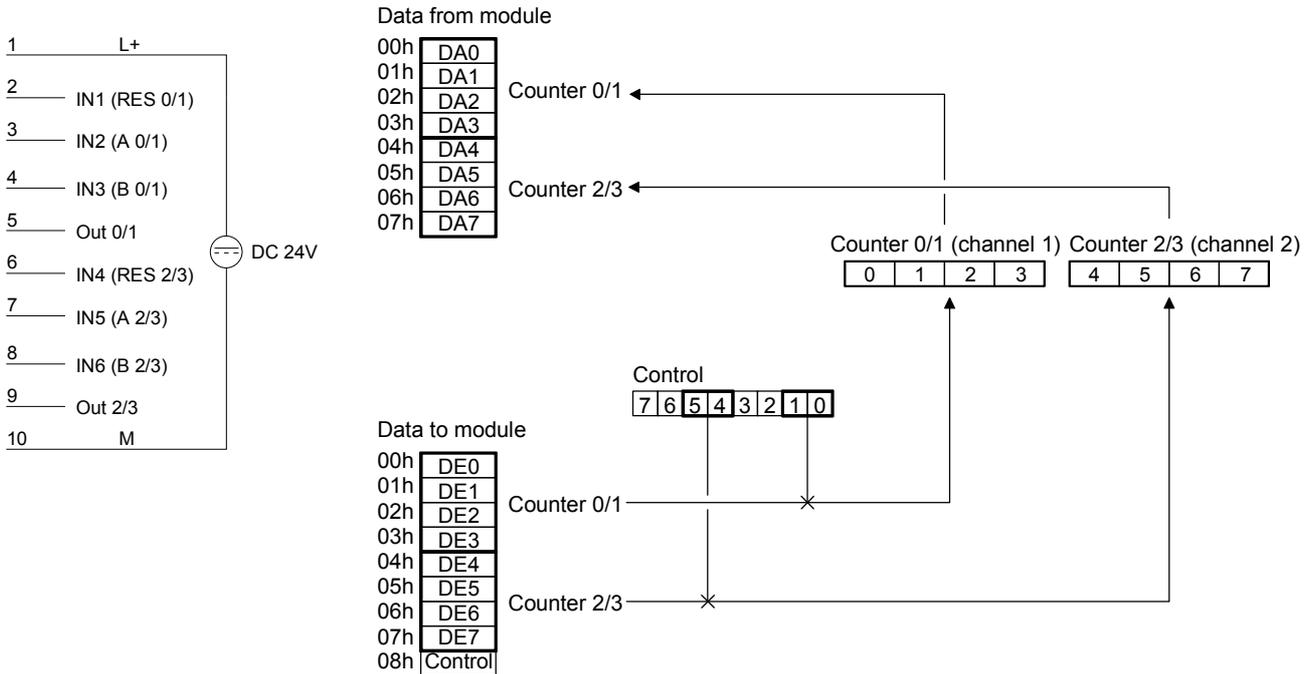
The counter is decremented by the rising edge of signal A if input B is at a HIGH level or by the falling edge of input A when input B is at a LOW level. Timing diagram for the counter 0/1 example:



**Mode 5  
Encoder 4 edges**

Every rising or falling edge at inputs A or B increments or decrements the counter. The direction depends on the level applied to the other input (B or A). RES has to be at a LOW level during the counting process. A HIGH level clears the counter. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero, the output remains active.

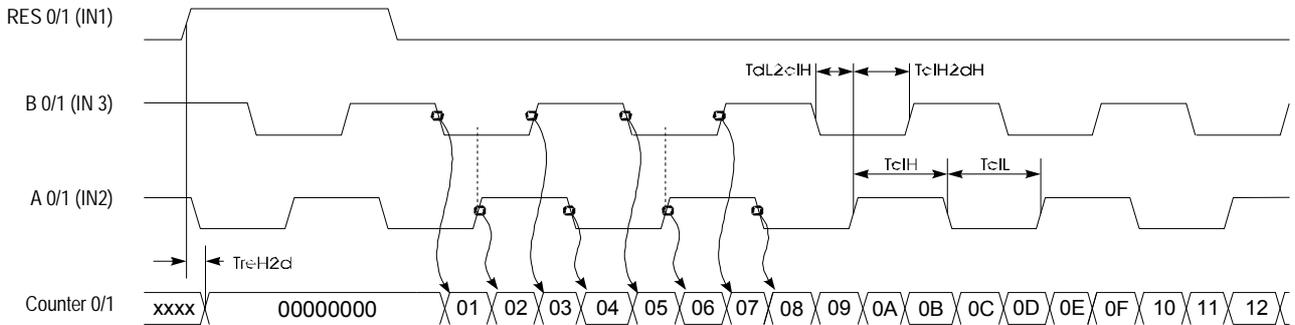
**Pin assignment  
access to counter**



**Up counter**

The counter is incremented when a rising edge is applied to B while input A is at a HIGH level or if a falling edge is applied to B when input A is at a LOW level. Alternatively it is also incremented when a rising edge is applied to A when input B is at a LOW level or by a falling edge at A when input B is at a HIGH level.

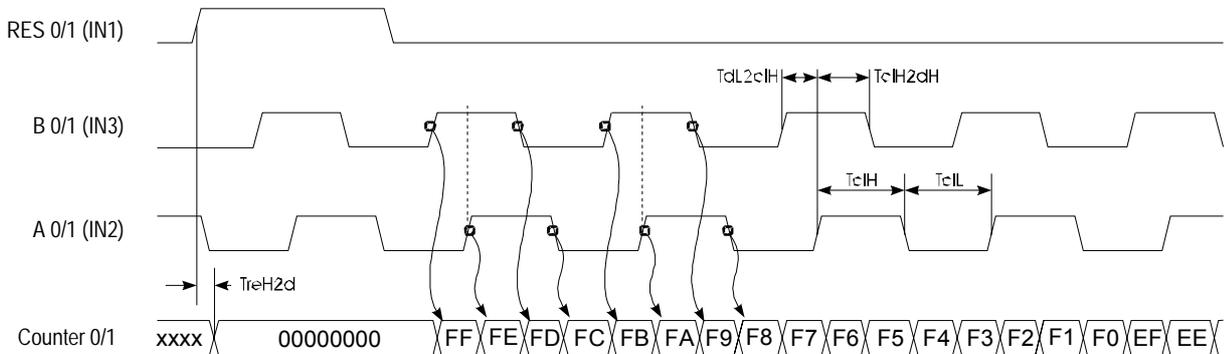
Timing diagram for the counter 0/1 example:



**Down counter**

The counter is decremented when a rising edge is applied to B while input A is at a LOW level or if a falling edge is applied to B when input A is at a HIGH level. Alternatively it is also decremented when a rising edge is applied to A when input B is at a HIGH level or by a falling edge at input A when input B is at a LOW level.

Timing diagram for counter 0/1 example:

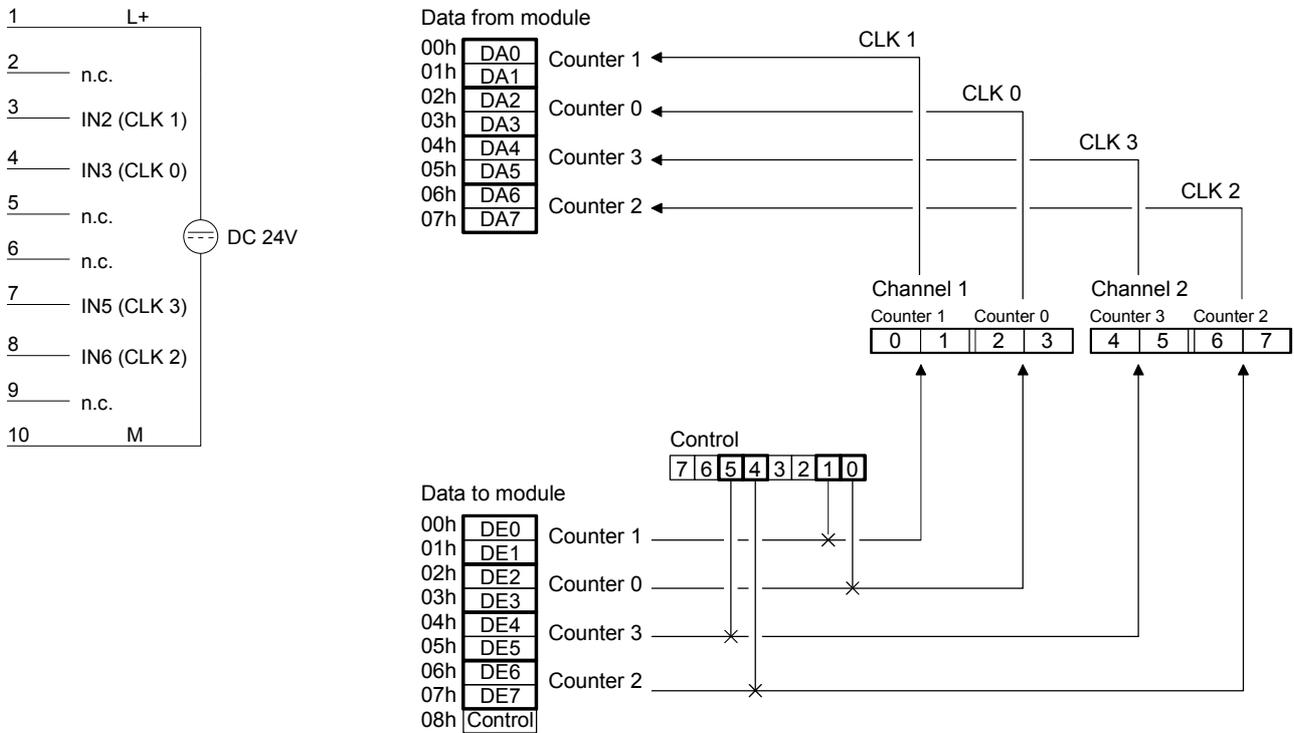


**Mode 8 ... 11  
two input counter  
function**

In this mode each channel provides 2 counters of 16Bit each. The rising edge of the input clock CLK x increments or decrements the respective counter. In this mode each counter can also be preset to a certain value by means of a control bit. Outputs are not available. A RESET is also not available. The following combinations are possible for every channel:

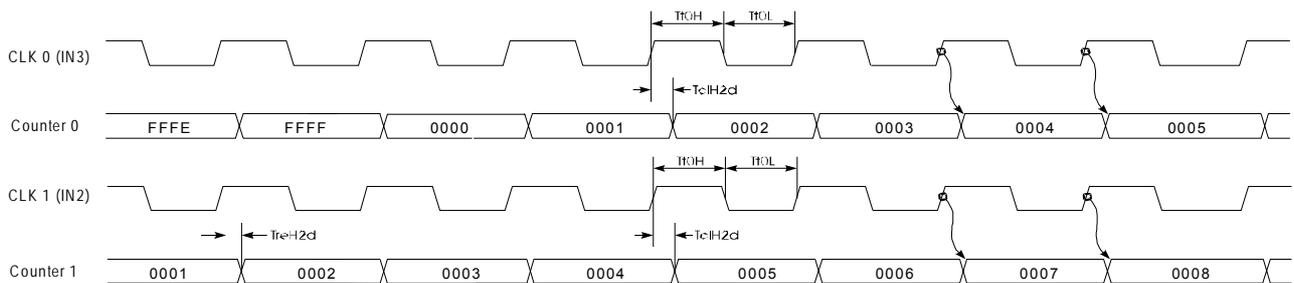
- Mode 8 - counter 0/1 up, counter 2/3 up**
- Mode 9 - counter 0/1 down, counter 2/3 up**
- Mode 10 - counter 0/1 up, counter 2/3 down**
- Mode 11 - counter 0/1 down, counter 2/3 down**

**Pin assignment  
access to counter**



**Timing diagram**

Below follows a timing diagram depicting an example of counter 0 and counter 1 in mode 8:



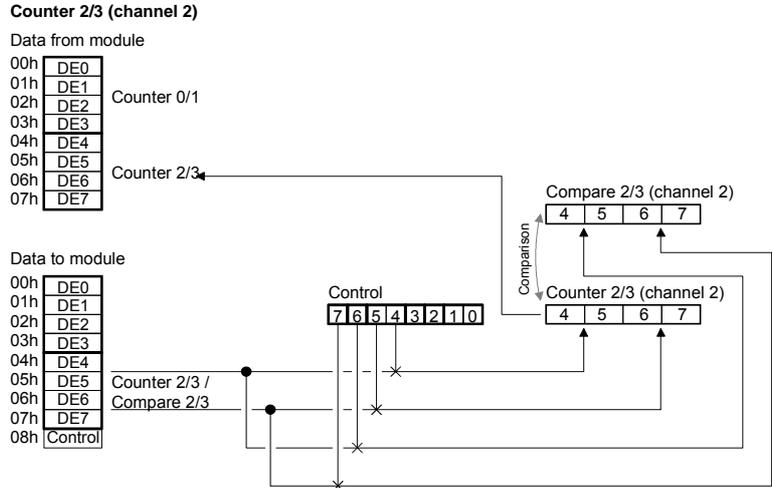
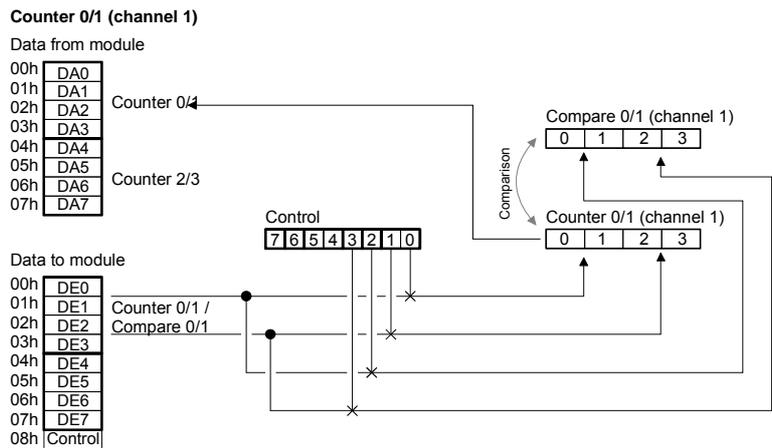
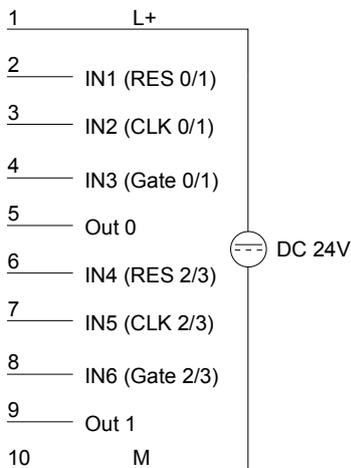
**Mode 12 and 13  
32bit counter with  
gate**

In mode 12 and mode 13 you can implement a 32Bit counter that is controlled by a gating signal (Gate). The direction of counting depends on the selected mode. Every rising edge of the input signal increments or decrements the counter provided that the GATE signal is at HIGH level. RES has to be LOW during the counting process. A HIGH level clears the counter. When the counter reaches the value that was previously loaded into the compare register, output OUT is set active for a minimum period of 100ms while the counter continues counting.

**Mode 12 - 32Bit counter up + gate with compare**

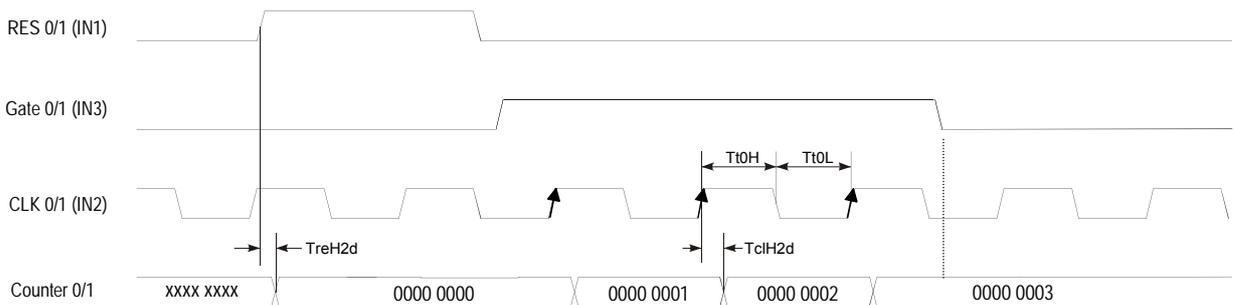
**Mode 13 - 32Bit counter down + gate with compare**

**Pin assignment access  
to counter**



**Timing diagram**

Below follows an example of a timing diagram of counter 0/1 in mode 12:



**Mode 14 and 15  
32Bit counter with  
gate and auto  
reload**

Modes 14 and 15 operate in the same manner as mode 12 and 13 with the addition of an Auto Reload function. The "Auto Reload" is used to define a value in the load register that is used to preset the counter automatically when it reaches the compare value.

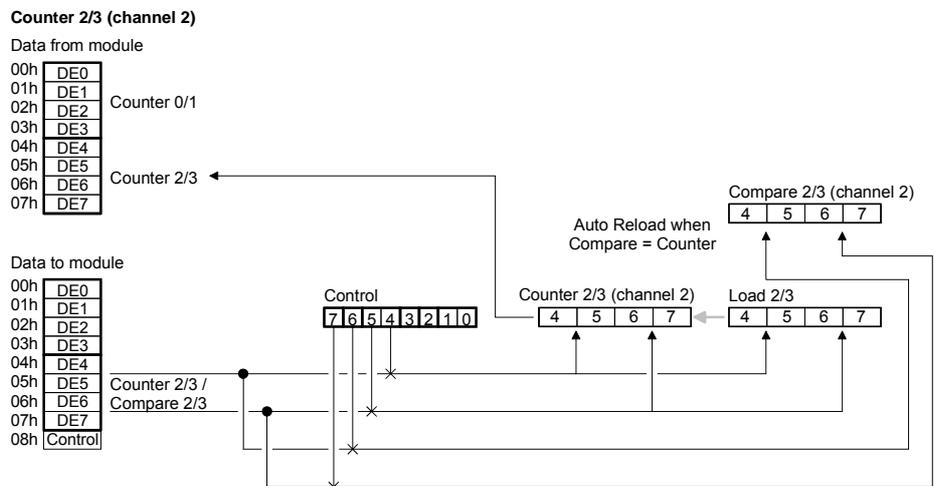
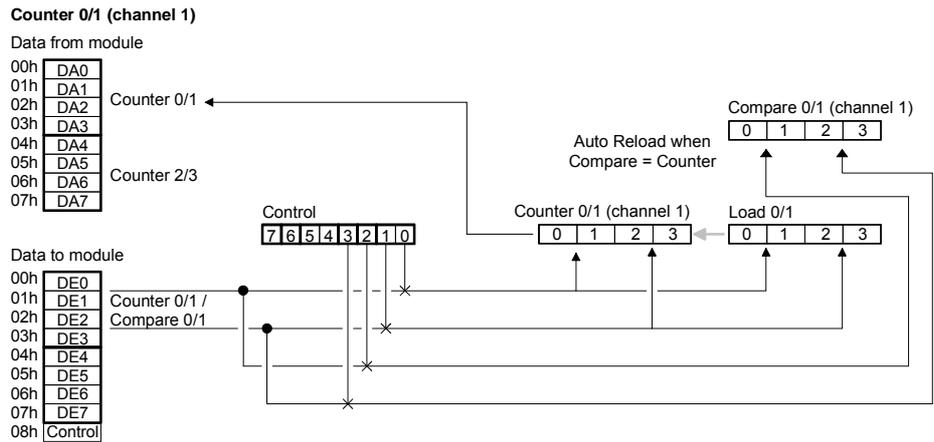
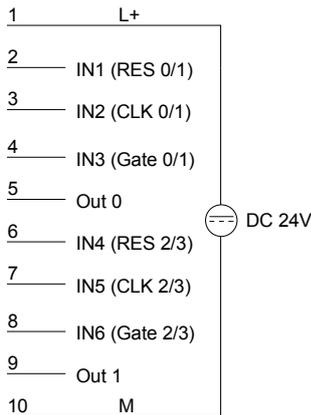
A HIGH pulse applied to RES clears the counter to 0000 0000. A HIGH level applied to GATE enables the counter so that is incremented/decremented by every rising edge of the CLK signal. As long as GATE is HIGH, the counter will count every rising edge of the signal applied to CLK until the count is one less than the value entered into COMPARE. The next pulse overwrites the counter with the value contained in the load register. This process continues until GATE is set to a LOW level. When an auto reload occurs, the status of the respective output changes.

The RES signal only resets the counter but not the outputs.

**Mode 14 - 32Bit counter up + gate with compare and auto reload**

**Mode 15 - 32Bit counter down + gate with compare and auto reload**

**Pin assignment  
access to counter**



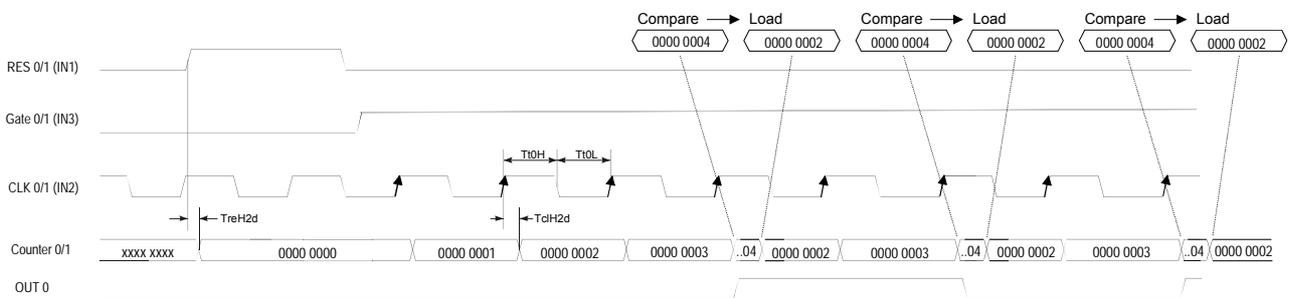
**Example**

This example is intended to explain the operation of the counters in mode 14 and 15.

A HIGH pulse applied to RES clears the counter to 0000 0000. A HIGH level applied to GATE enables the counter. As long as GATE is HIGH the counter will count every rising edge of the signal applied to CLK until the count is one less than the value entered into COMPARE. In this example the counter counts to 0000 0004 followed immediately by an auto reload, i.e. the counter is preset to the contents of the load register (in this case 0000 0002). The state of output OUT 0 changes every time an auto reload is executed.

In this example the counter counts from 0000 0002 to 0000 0004 as long as the GATE input is at a HIGH level.

Every load operation changes the status of output OUT 0.



**Mode 16  
frequency  
measurement**

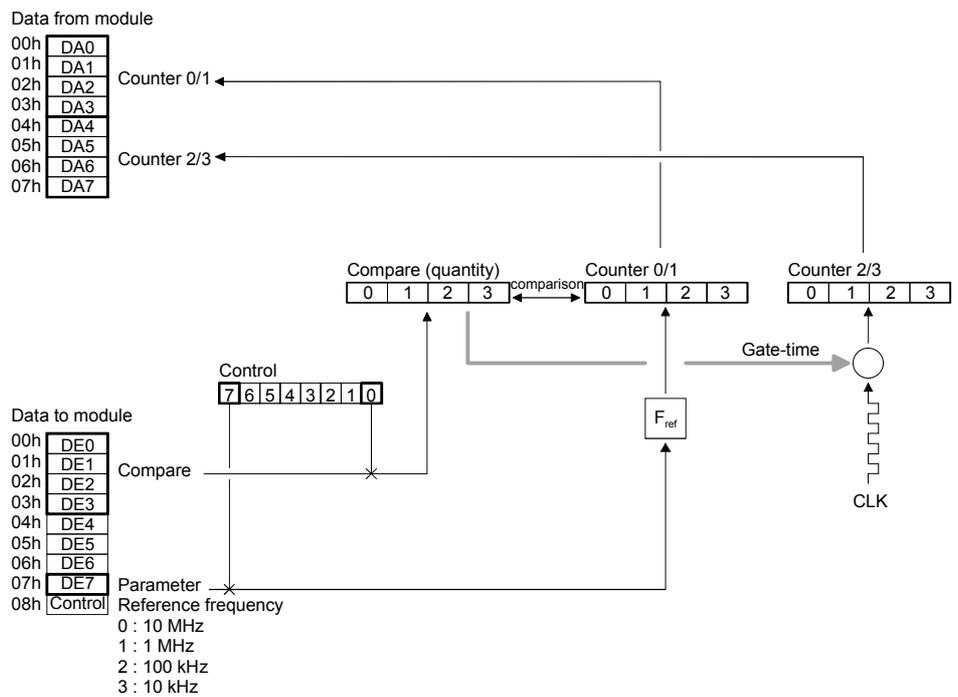
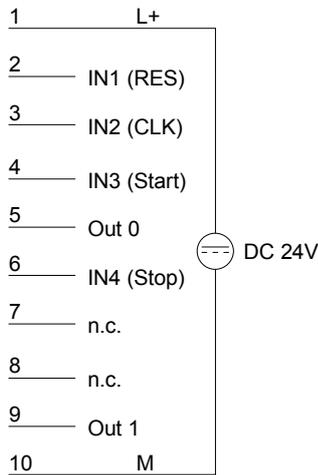
In this mode it is possible to determine the frequency of the signal that is applied to the CLK input. Counter 0/1 is provided with a reference signal by means of DE7 and a gate time that is controlled indirectly by the value n to determine the duration for which counter 2/3 is enabled. The value of n has a range from 1 to 2<sup>32</sup>-1 and it is loaded into the COMPARE register.

When enabled by the rising edge of the signal applied to Start, counter 0/1 counts reference pulses of the reference clock generator from the first rising edge of the CLK signal.

During this time counter 2/3 counts every rising edge of the CLK signal. Both counters are stopped when counter 0/1 reaches the COMPARE value or when a HIGH level is applied to Stop. You may calculate the frequency by means of the formula shown below.

*This mode can not be combined with other modes!*

**Pin assignment  
access to counter**



**Frequency  
calculation**

When the measurement has been completed you may calculate the frequency as follows:

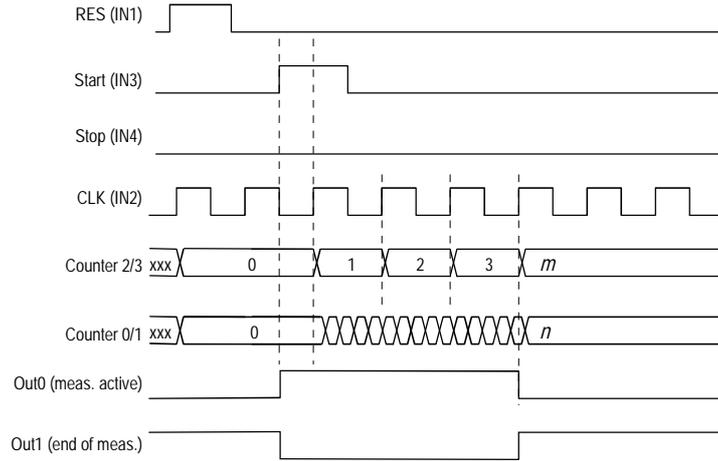
$$Frequency = \frac{F_{ref} \cdot m}{n}$$

where *F<sub>ref</sub>*: reference frequency (supplied in DE7 with control bit 7)

*m*: counter 2/3 contents (number of CLK pulses)

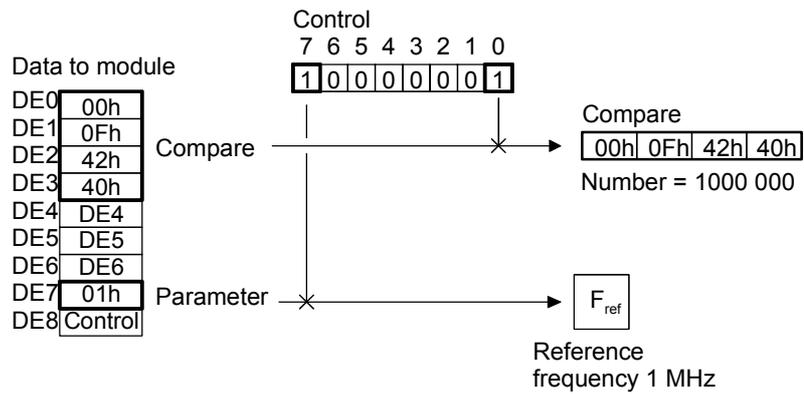
*n*: number of reference frequency pulses in counter 0/1 (equal to COMPARE, if the operation was not terminated prematurely by means of Stop)

**Timing diagram**



**Example**

Quantity = 1 000 000 pulses  
Reference frequency = 1MHz



Using a frequency of 1MHz and 1 000 000 pulses will return 1Hz, i.e. when the measurement is completed, counter 2/3 contains the frequency directly - no conversion is required.



**Note!**

Counter 2/3 will indicate the exact frequency if you choose  $F_{ref}$  and  $n$  so that the formula returns 1Hz precisely.

**Mode 17  
period  
measurement**

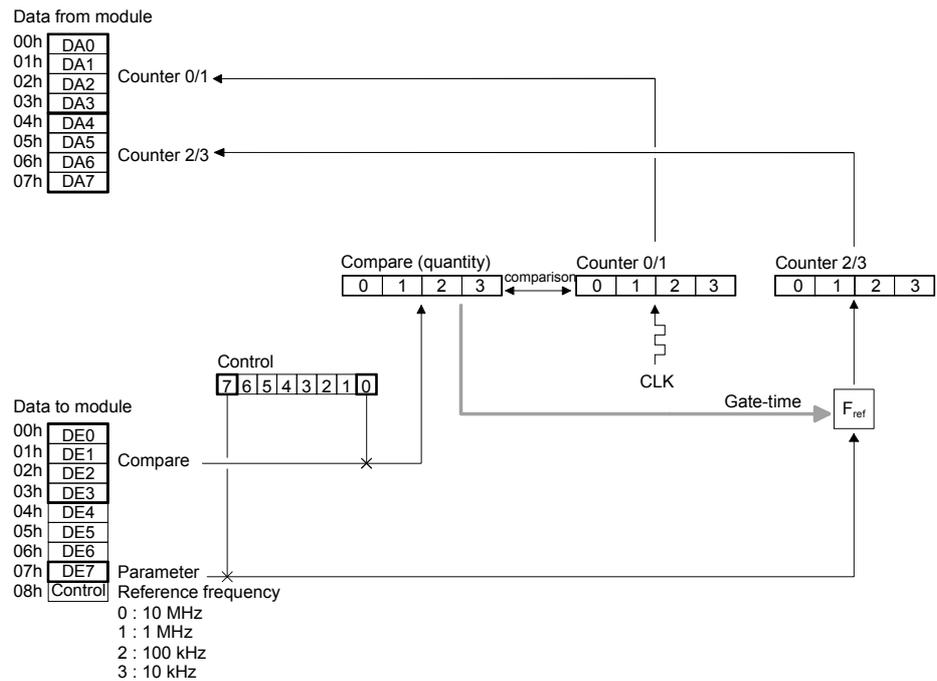
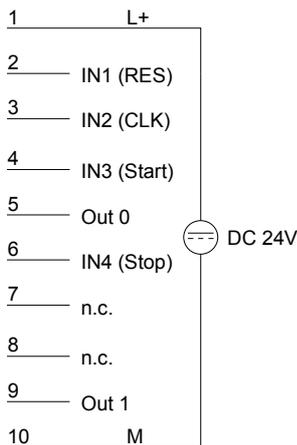
This mode is used to determine the average period of n measuring intervals of a signal that is connected to the CLK input. For this purpose you supply a reference clock to counter 2/3 by means of DE7 and indirectly a gate time defined by the value of n for which counter 2/3 is enabled. The value of n has a range from 1 to  $2^{32}-1$  and it is loaded into the COMPARE register.

The measurement period begins when a rising edge is applied to Start. During this period counter 2/3 counts reference pulses from the reference clock generator starting with the first rising edge of the CLK signal.

In the mean time counter 0/1 counts every rising edge of the CLK signal. Both counters are stopped when the count in counter 0/1 reaches the Compare value or when Stop is set to a HIGH level. You may then calculate the average period by means of the formula shown below.

*This mode can not be combined with other modes!*

**Pin assignment  
access to counter**



**Period calculation** When the measurement has been completed, you may calculate the period as follows:

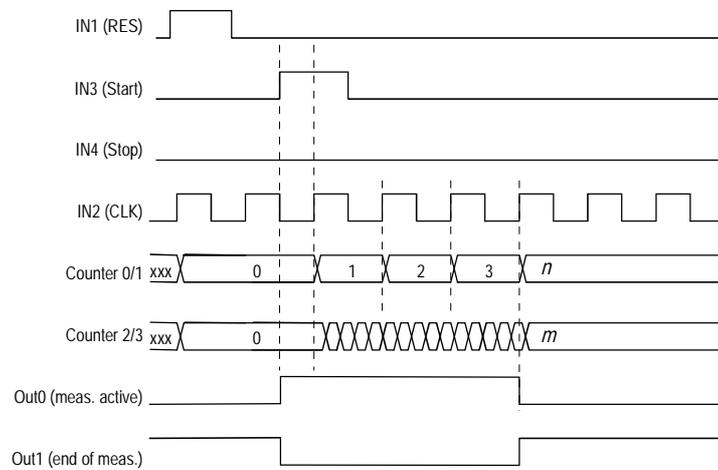
$$Period = \frac{m}{Fref \cdot n}$$

where *Fref*: reference frequency (supplied in DE7 with control bit 7)

*m*: contents of counter 2/3 (counts reference clock pulses)

*n*: number of CLK pulses in counter 0/1 (corresponds to COMPARE, provided it was not terminated prematurely by Stop)

**Timing diagram:**

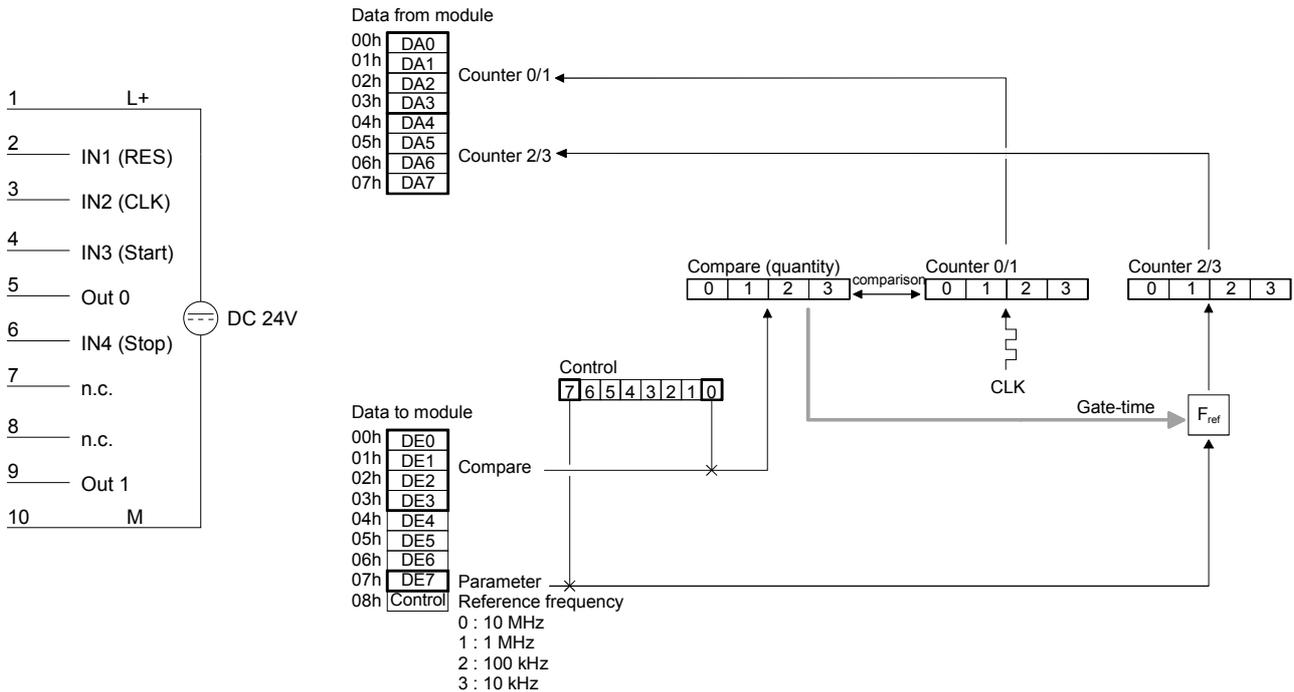


**Mode 18  
frequency  
measurement with  
gate output**

The operation of mode 18 is similar to mode 16. The only difference is the manner in which OUT 0 and OUT 1 are controlled. In this case OUT 0 is only activated when the counting operation starts and it is deactivated when counting ends, i.e. OUT 0 provides an indication of the internal gate. OUT 1 provides the inverted status of the gate.

*This mode can not be combined with other modes!*

**Pin assignment  
access to counter**



**Frequency  
calculation**

When the measurement has been completed, you may calculate the frequency as follows:

$$Frequency = \frac{F_{ref} \cdot m}{n}$$

- where *Fref*: reference frequency (supplied in DE7 with control bit 7)
- m*: contents of counter 2/3 (CLK pulse count)
- n*: number of pulses of the reference frequency in counter 0/1 (corresponds to COMPARE provided it was not terminated prematurely by Stop)

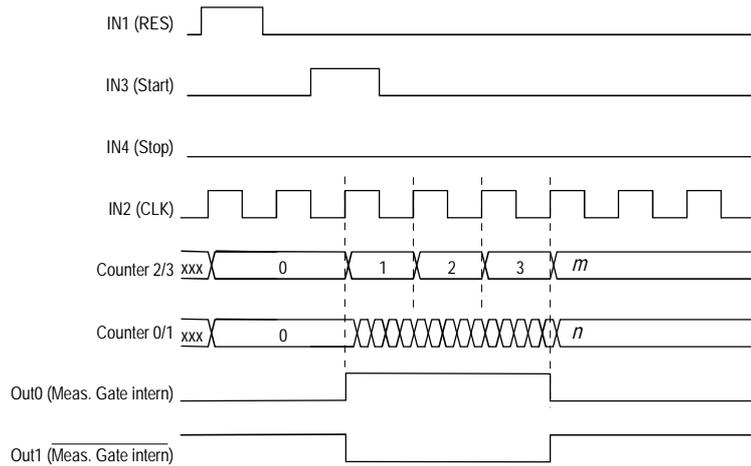


**Note!**

Counter 2/3 will indicate the exact frequency if you choose  $F_{ref}$  and  $n$  so that the formula returns 1Hz precisely.

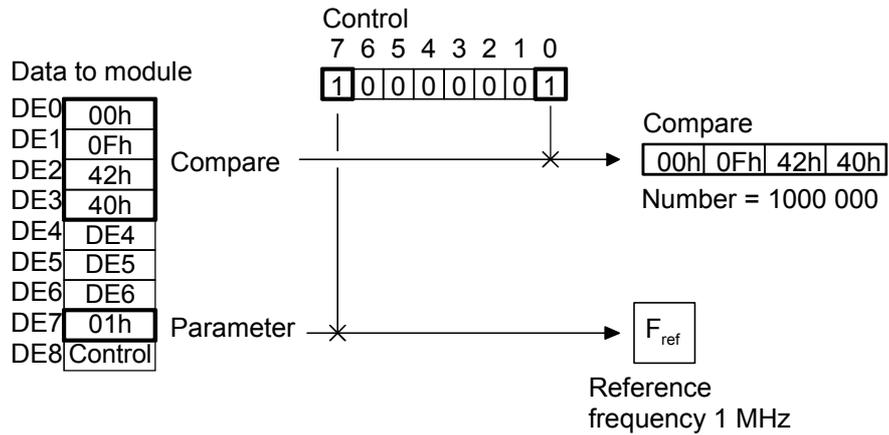
For example when the applied frequency is 1MHz and the number of pulses is 1 000 000 the result will be 1Hz, i.e. counter 2/3 contains the precise frequency after the measurement - this does not require further conversion.

**Timing diagram:**



**Example**

Pulse count = 1 000 000  
Reference frequency = 1MHz

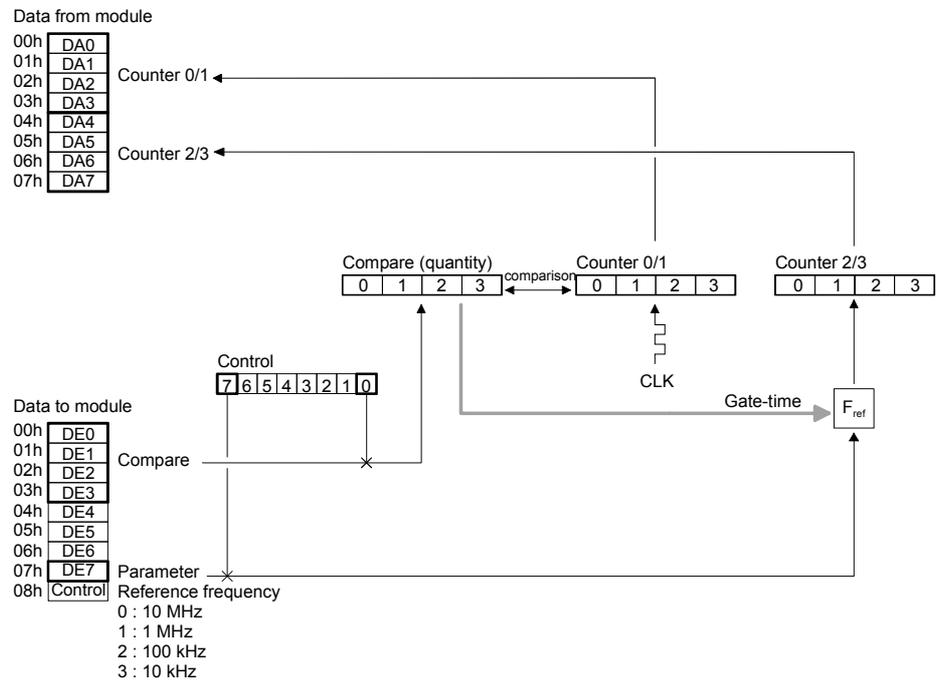
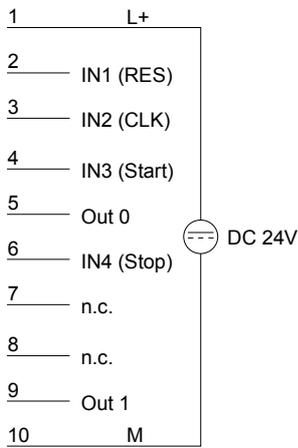


**Mode 19  
period  
measurement with  
gate output**

The operation of mode 19 is identical to mode 17. The only difference is the manner in which OUT 0 and OUT 1 are controlled. Other than for mode 17, OUT 0 is only activated when the counting operation starts and it is deactivated when counting ends, i.e. OUT 0 provides an indication of the internal gate. OUT 1 provides the inverted status of the gate.

*This mode can not be combined with other modes!*

**Pin assignment  
access to counter**



**Period calculation** When the measurement has been completed you may calculate the mean period as follows:

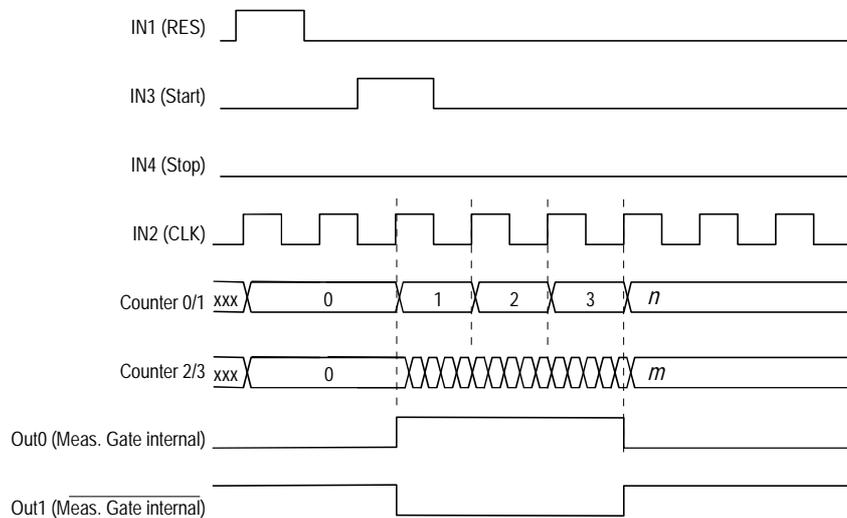
$$Period = \frac{m}{Fref \cdot n}$$

where *Fref*: reference frequency (supplied in DE7 with control bit 7)

*m*: contents of counter 2/3 (reference clock pulse count)

*n*: number of CLK pulses in counter 0/1 (corresponds to COMPARE, provided it was not terminated prematurely by Stop)

**Timing diagram:**



**Mode 6  
pulse measuring,  
Pulse LOW, 50kHz  
with direction  
control**

The pulse width of a signal connected to the CLK input is determined by means of an internal time base and saved. The measurement is started with the falling edge of the input signal and it is stopped by the rising edge of the input. This saves the value in 20µs units in a buffer from where it may be retrieved (corresponds to Fref = 50kHz).

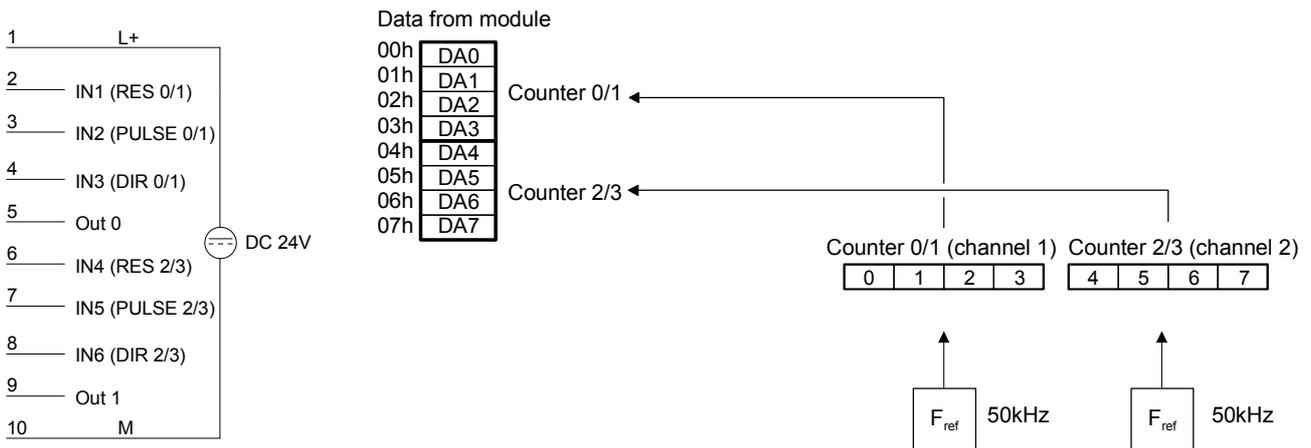
Input DIR determines the counting direction of the counter. If DIR is at a LOW level the counter counts up. A HIGH level lets the counter count down.

The input RES has to be at a LOW level. A HIGH at this input would clear the counter.

With the rising edge of the signal pulse, a result is transferred into the DA area; the result remains available until it is overwritten by the next new result.

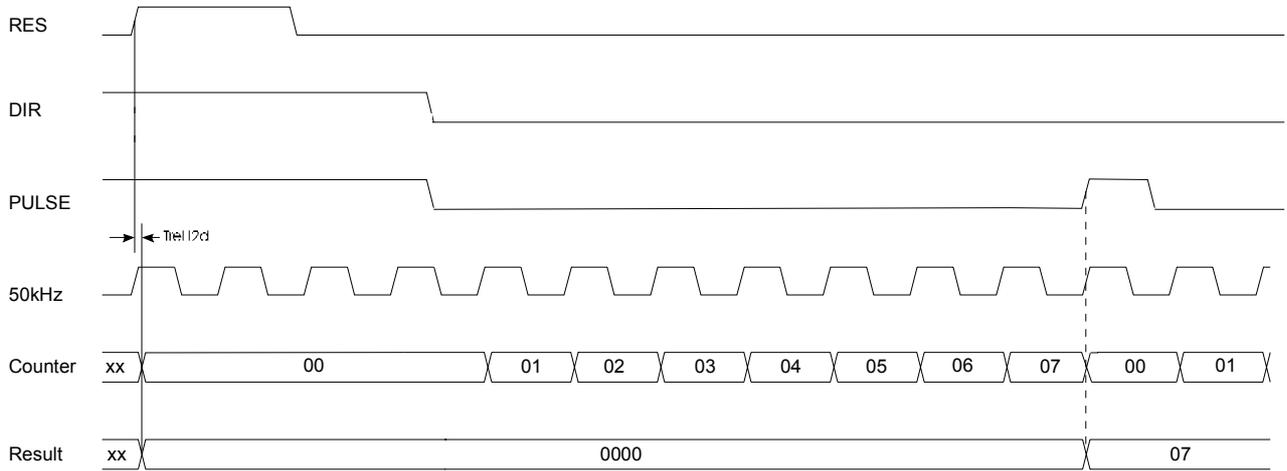
Signals Out 0 or Out 1 are not modified.

**Pin assignment  
access to counter**



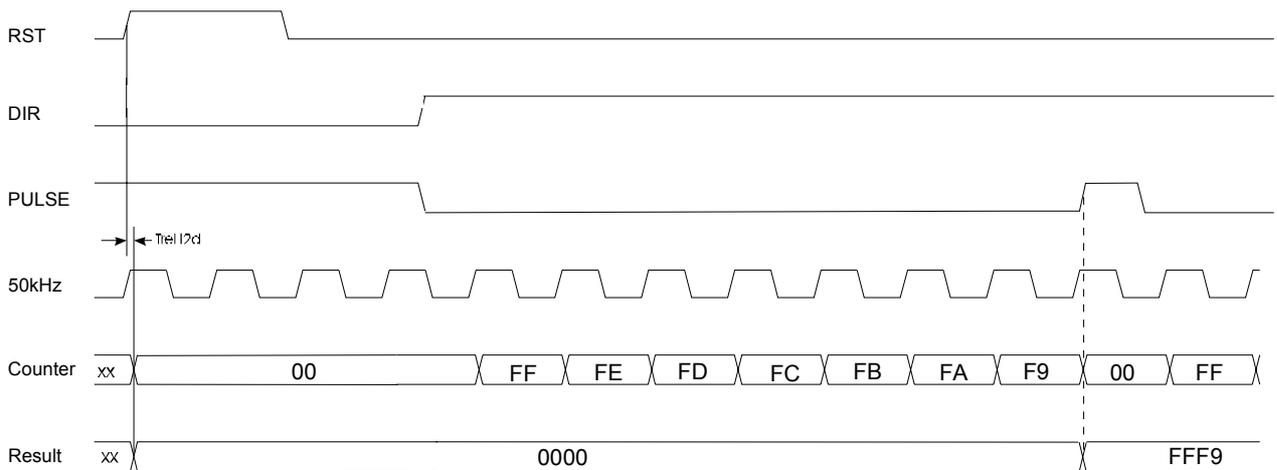
**Up counter**

The RES signal and the DIR signal are reset. The measurement is started by the falling edge at input PULSE and the counter is clocked up by the 50kHz clock. The rising edge of the signal at input PULSE terminates the count operation and the result is transferred into the result register. The result is available to the PLC. The value remains in the result register until a new measurement has been completed which overwrites the register.



**Down counter**

The RES signal is reset and the DIR signal is placed at a HIGH level. The measurement is started by the falling edge at input PULSE and the counter is clocked down by the 50kHz clock. The rising edge of the signal at input PULSE terminates the count operation and the result is transferred into the result register. The result is available to the PLC. The value remains in the result register until a new measurement has been completed which overwrites the register.



**Mode 20  
pulse  
measurements,  
pulse down**

**prog. time base with direction control**

The pulse width of a signal that is applied to the PULSE input is determined by means of an internal time base. The measurement is started by the falling edge of the input signal and ends with the rising edge. The rising edge of the measured signal stores the resulting pulse width in units of  $1/F_{ref}$ , that may be retrieved again.

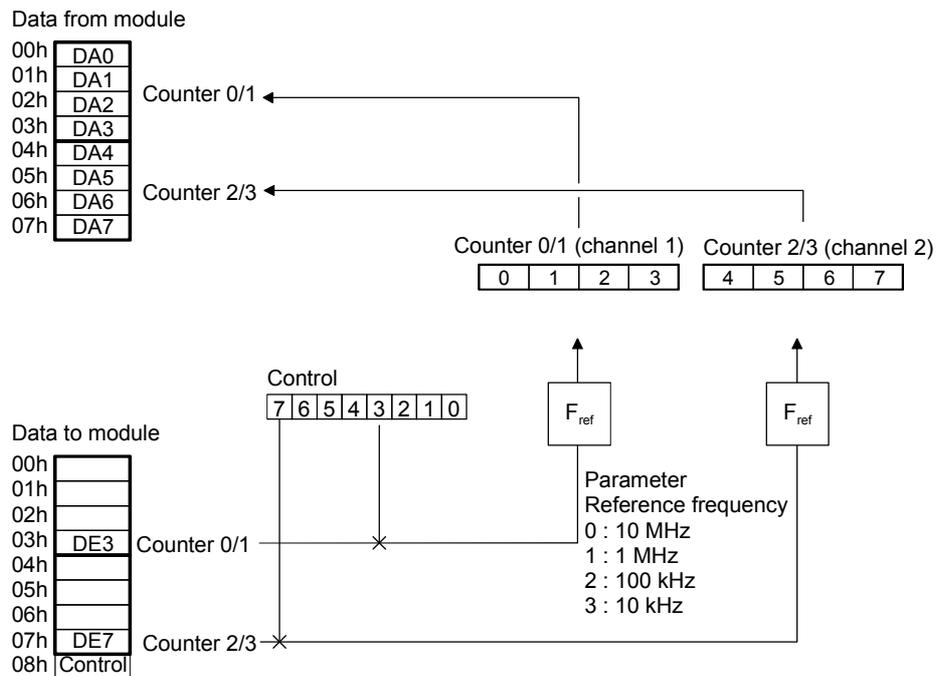
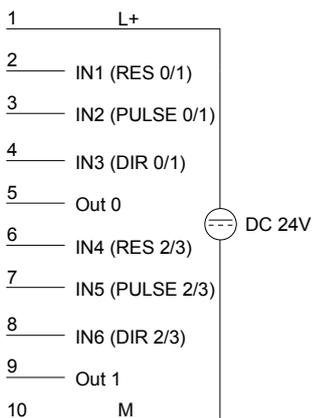
Input DIR controls the direction of the count. When DIR is held at a LOW level the counter counts up. When DIR is at a HIGH level the counter counts down.

RES has to be held at LOW during the counting operation. A HIGH level clears the counter.

Fref is programmable.

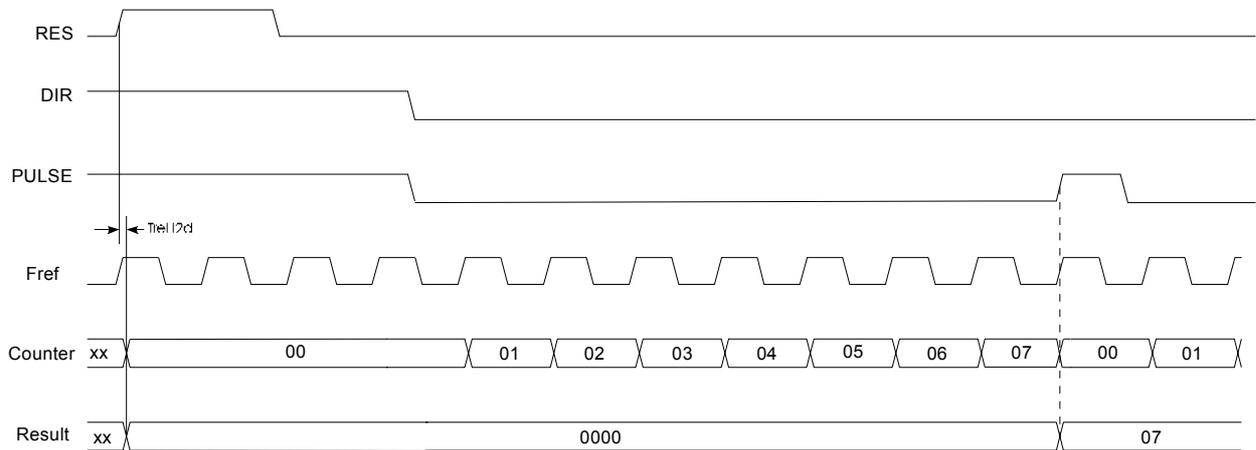
The OUT signal is not changed.

**Pin assignment  
access to counter**



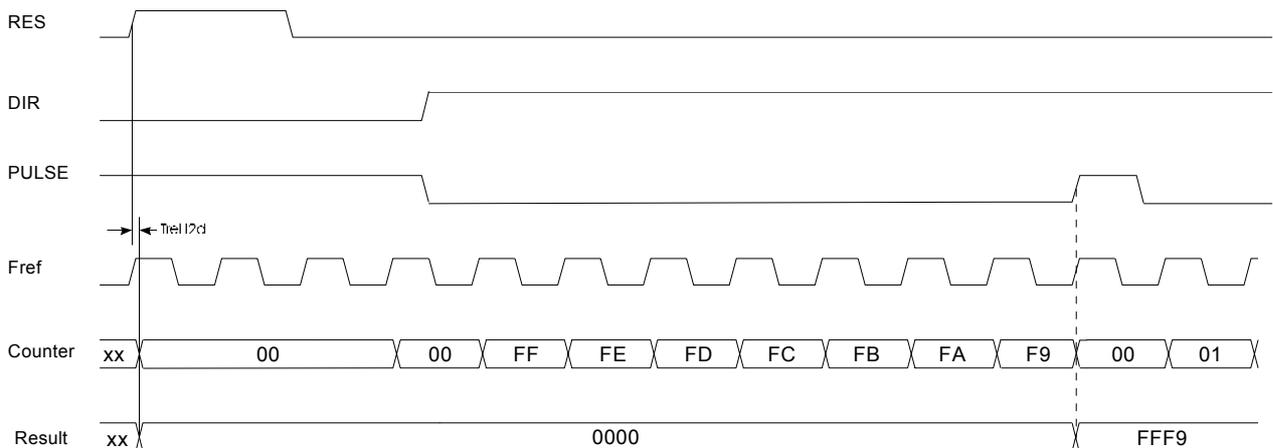
**Up counter**

The RES signal and the DIR signal are set to LOW. Subsequently the measurement is started with the falling edge of PULSE and the counter counts up in accordance with the selected time base. A rising edge at PULSE terminates the counting operation and the accumulated count is transferred into the result register. The result register is available to the PLC. The value remains in the result register until a new measurement has been completed and the register is changed by the new result.



**Down counter**

The RES signal is set to LOW and the DIR signal to HIGH. Subsequently the measurement is started with the falling edge of PULSE and the counter counts down in accordance with the selected time base. A rising edge at PULSE terminates the counting operation and the accumulated count is transferred into the result register. The result register is available to the PLC. The value remains in the result register until a new measurement has been completed and the register is changed by the new result.



**Mode 21  
pulse  
measurement,  
pulse low**

**Direction up, prog. time base, with release**

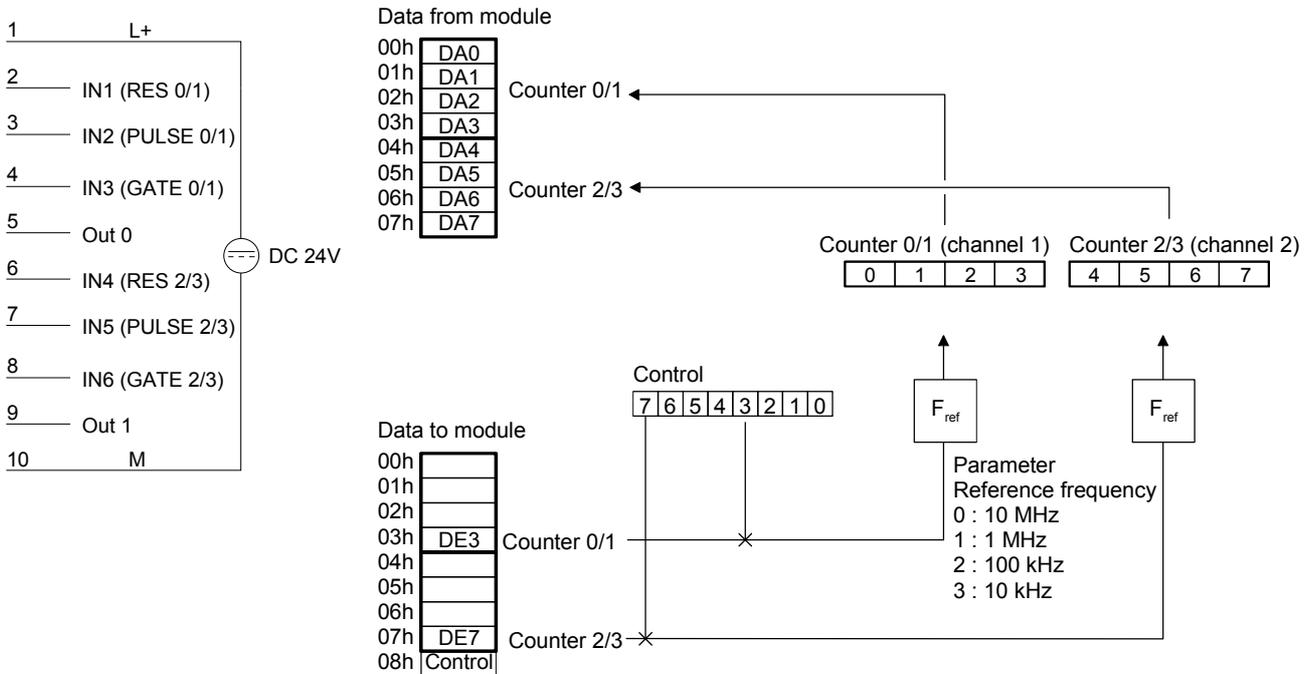
The pulse width of a signal applied to the PULSE input is determined by means of a programmable time base (Fref). The measurement starts with the falling edge of the input signal and it is stopped by the rising edge of the input signal. The rising edge of the input signal saves the resulting pulse width in units of 1/Fref. This is available to other devices.

A condition for the function is that a HIGH level is applied to the GATE input.

Input RES must be at a LOW level. A HIGH level at this input would clear the counter.

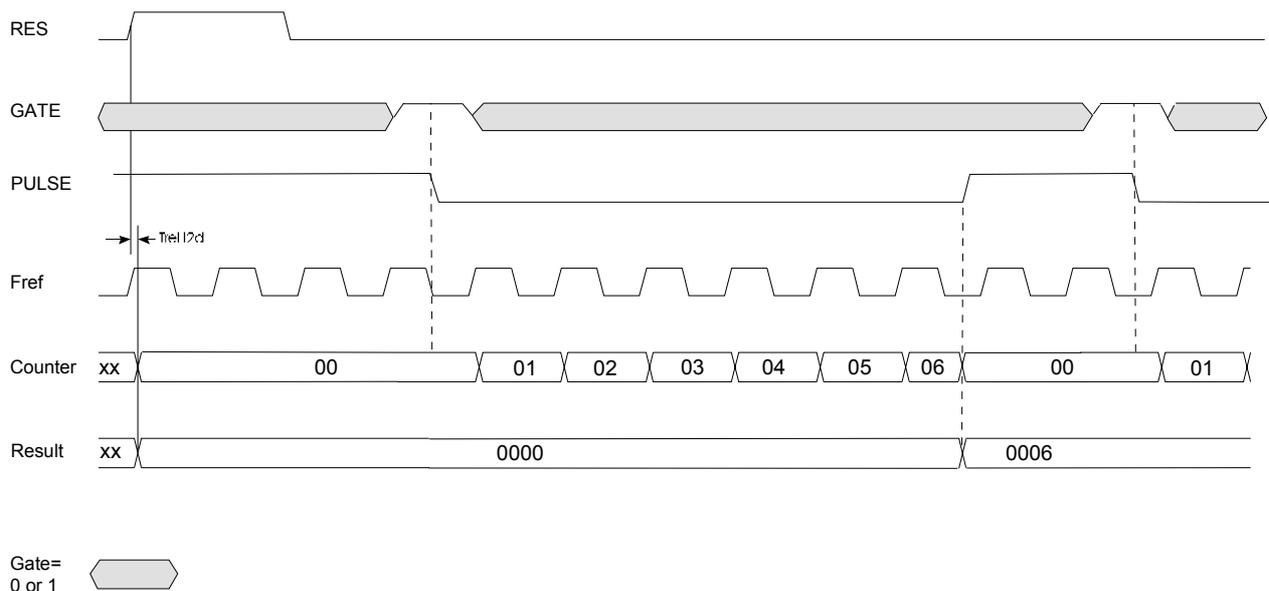
The OUT signal is not modified.

**Pin assignment  
access to counter**



**Up counter**

The RES signal is set to zero. The measurement can only be started when the GATE signal is at a HIGH level. The measurement is started with the falling edge of PULSE and the counter counts up in accordance with the selected time base. A rising edge at PULSE terminates the counting operation and the accumulated count is transferred into the result register. The result register is available to the PLC. The value remains in the result register until a new measurement has been completed and the register is changed by the new result.



**Mode 22  
pulse  
measurement,  
pulse high**

**Direction up, programmable time base, with release**

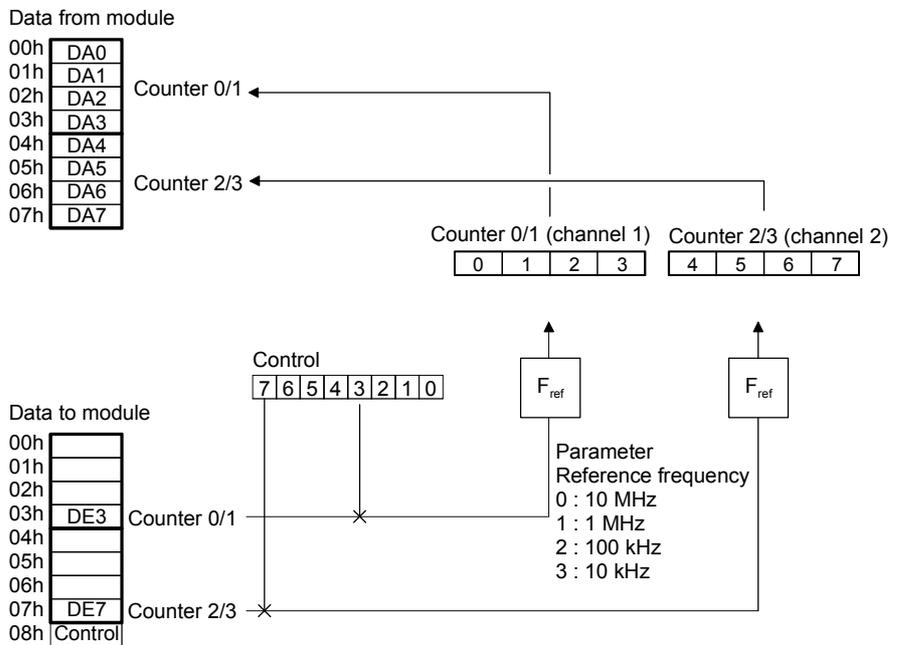
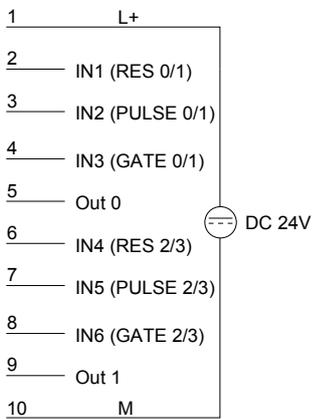
The pulse width of a signal applied to the PULSE input is determined by means of a programmable time base (Fref). The measuring starts with the rising edge of the input signal and ends with the falling edge. The rising edge of the input signal saves the resulting pulse width in units of 1/Fref. This is available to other devices.

A condition for the function is that a HIGH level is applied to the GATE.

Input RES must be at a LOW level. A HIGH level at this input would clear the counter.

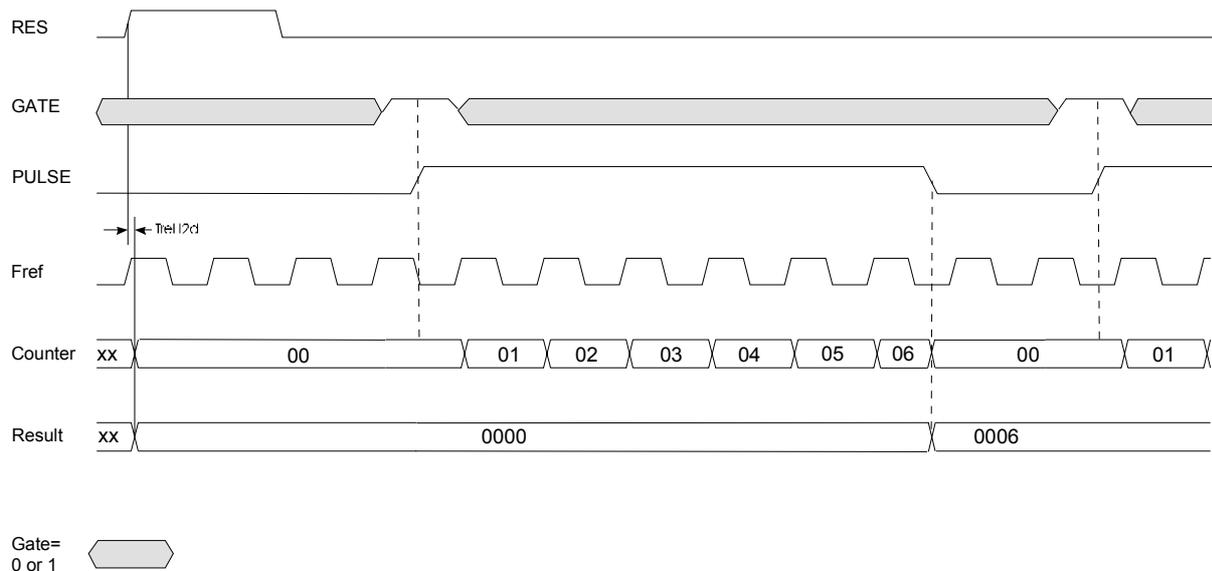
The OUT signal is not modified.

**Pin assignment  
access to counter**



### Up counter

The RES signal is set to zero. The measuring only starts if the GATE signal is set to HIGH with the rising edge at PULSE. A falling edge at PULSE terminates the counting operation and the accumulated count is transferred into the result register. The result register is available to the PLC. The value remains in the result register until a new measurement has been completed and the register is changed by the new result.

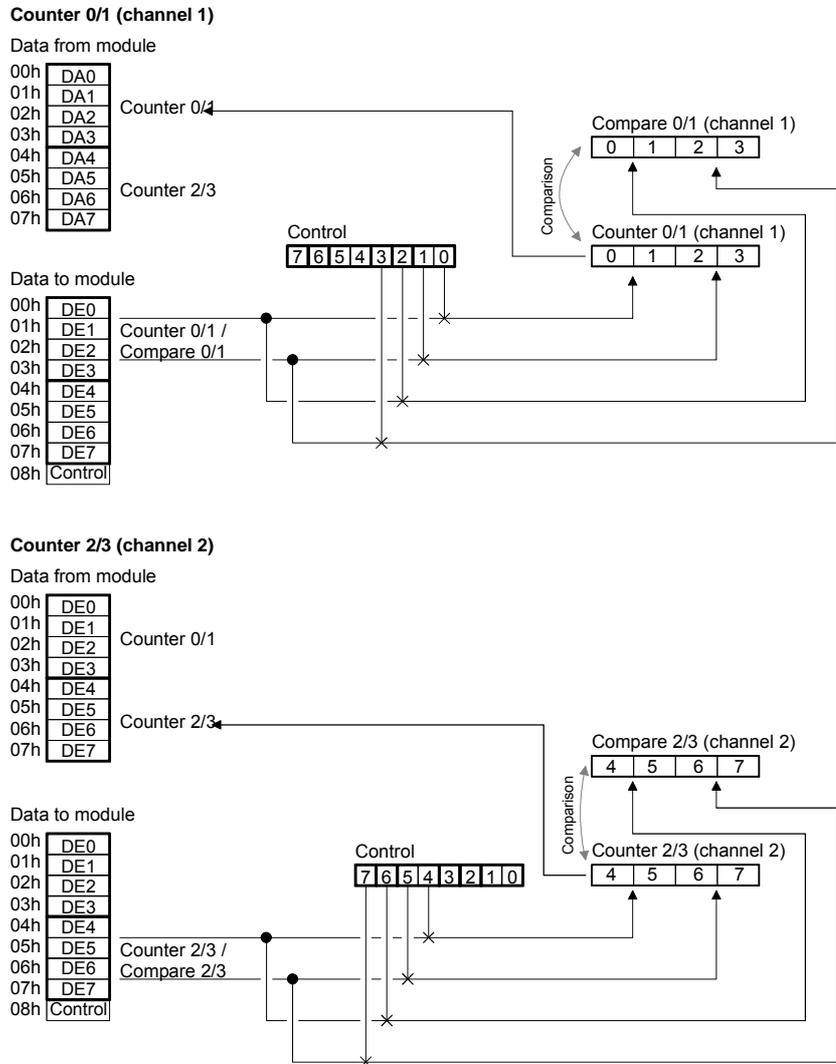
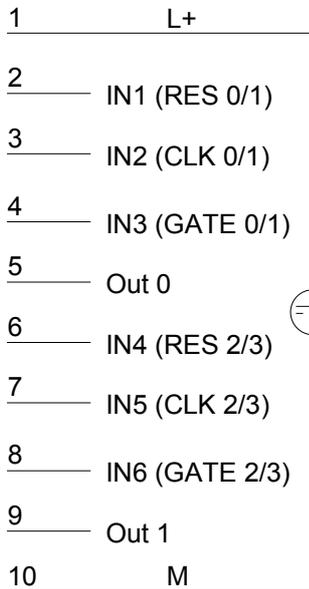


**Mode 23**  
**One Shot, count up, with release, output signal**

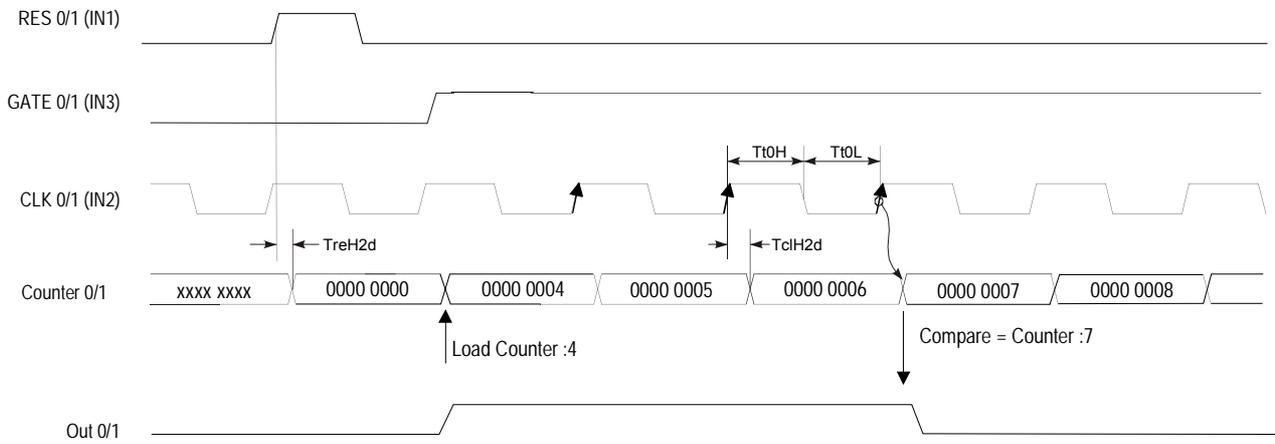
In mode 23 you may implement one 32Bit counter per channel, each one controlled by a GATE signal. Every rising edge of the input clock increments the counter by 1 as long as the signal applied to GATE is HIGH. RES must be at a LOW level. A HIGH level clears the counter. The counter is started by loading. Starting the counter, the output OUT is set active (HIGH). OUT is cleared when the value entered into COMPARE is reached. The counter will continue the count operation after the value in COMPARE was reached.

**Mode 23 - One Shot, up with Gate input, Output set**

**Pin assignment access to counter**



**Timing diagram** Example of counter 0/1 in mode 23:

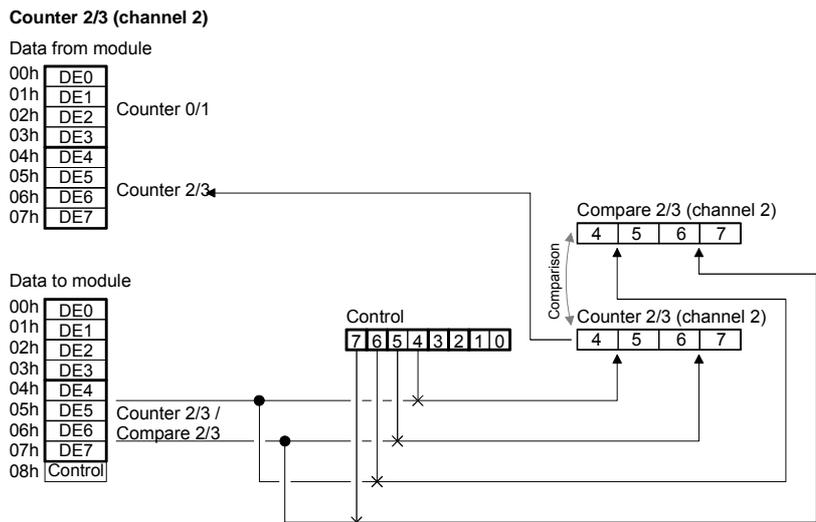
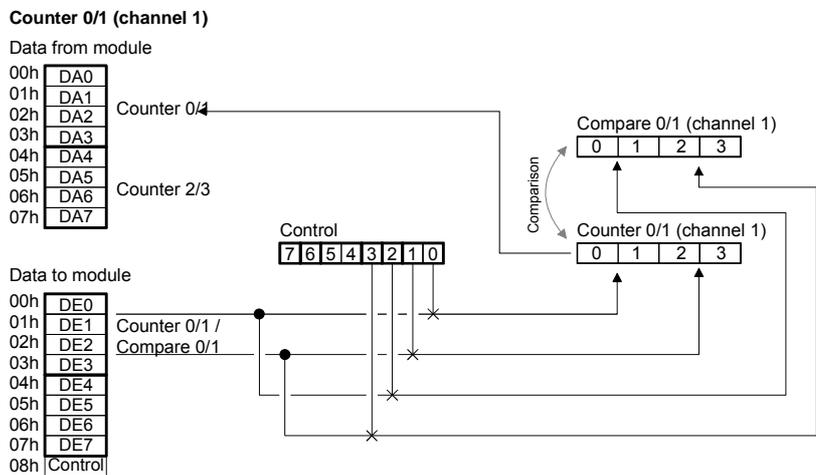
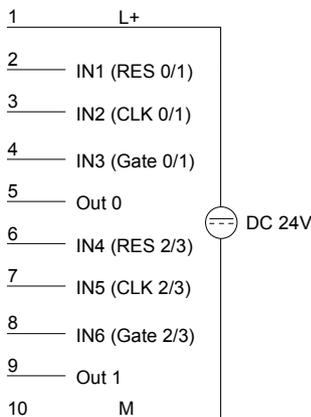


**Mode 24**  
**One Shot, count down, with gate, output signal**

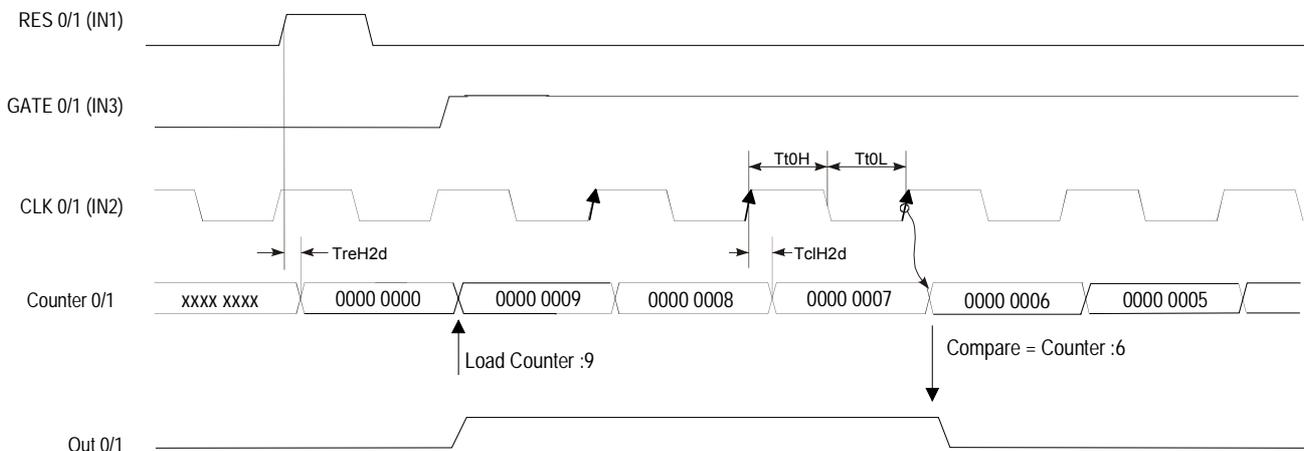
In mode 24 you may implement one 32Bit counter per channel, each one controlled by the signal applied to the GATE input. Every rising edge of the input clock decrements the counter by 1 as long as the signal applied to GATE is HIGH. RES must be at a LOW level. A HIGH level at this input would clear the counter. The counter is started by loading. Starting the counter, the output OUT is set active (HIGH). OUT is cleared when the value entered into COMPARE is reached. The counter will continue the count operation after the value in COMPARE was reached.

**Mode 24 - One Shot, down with Gate-Input, Output set**

**Pin assignment access to counter**



**Timing diagram** Example of counter 0/1 in mode 24:

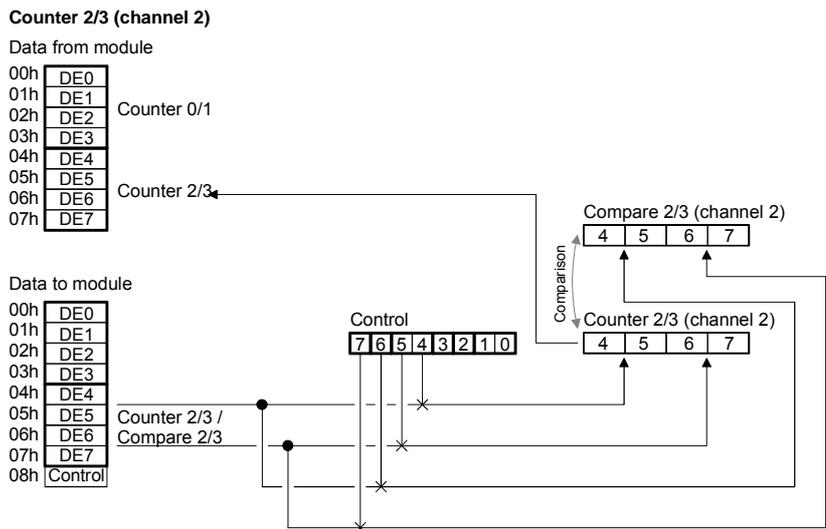
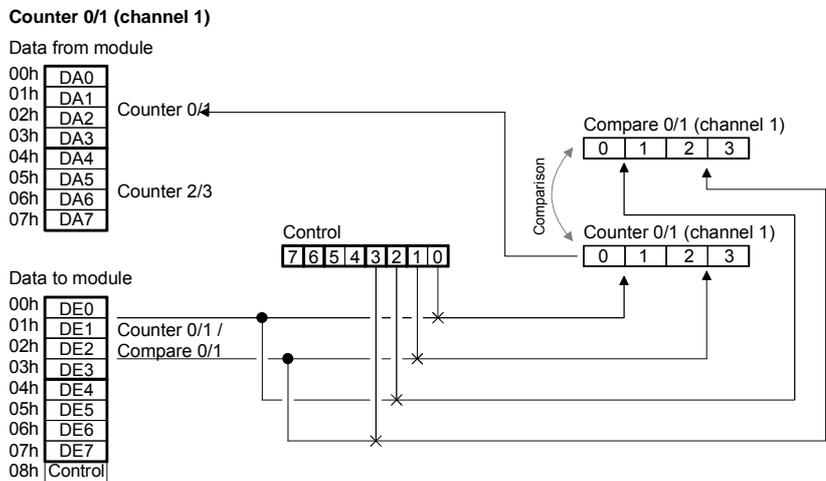
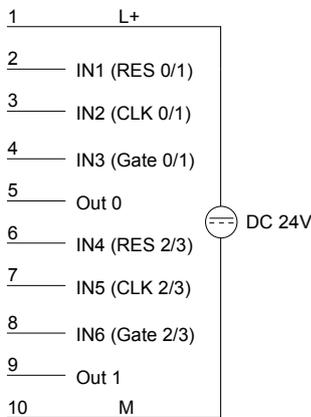


**Mode 25  
One Shot, count up, with reset signal**

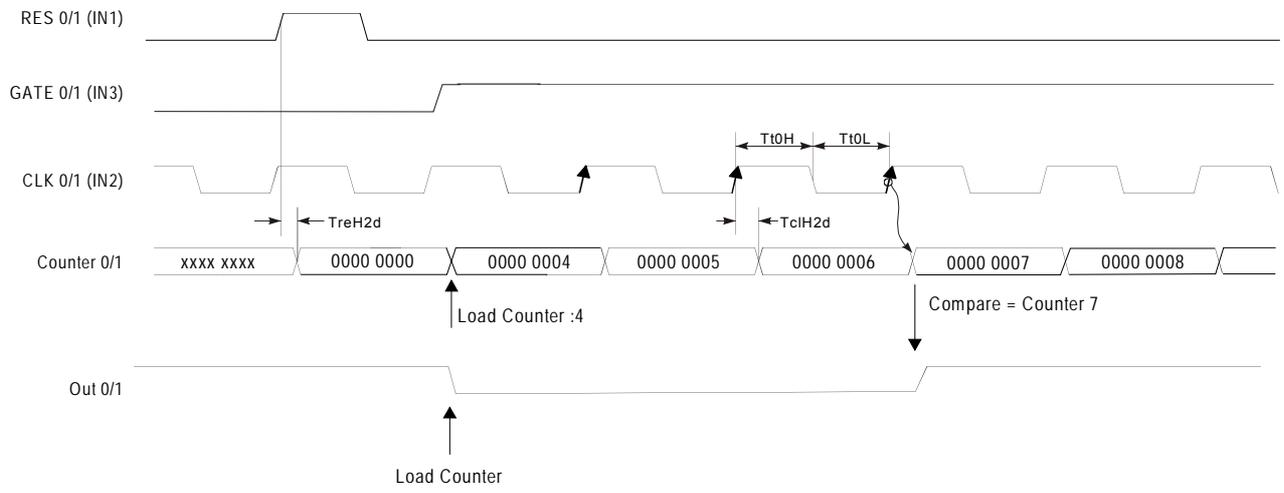
In mode 25 you may implement one 32Bit counter per channel, each one controlled by the signal applied to the GATE input. Every rising edge of the input clock increments the counter by 1 as long as the signal applied to GATE is HIGH. RES must be at a LOW level. A HIGH level at this input would clear the counter. The counter is started by loading. Starting the counter, the output OUT is set active (LOW). OUT becomes HIGH when the value entered into COMPARE is reached.

**Mode 25 One Shot, count up, Reset**

**Pin assignment  
access to counter**



**Timing diagram** Example of counter 0/1 in mode 25:

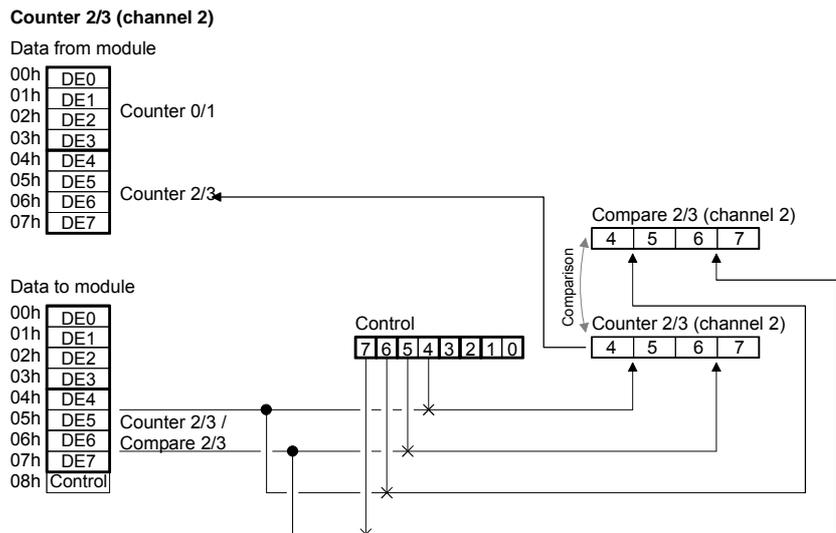
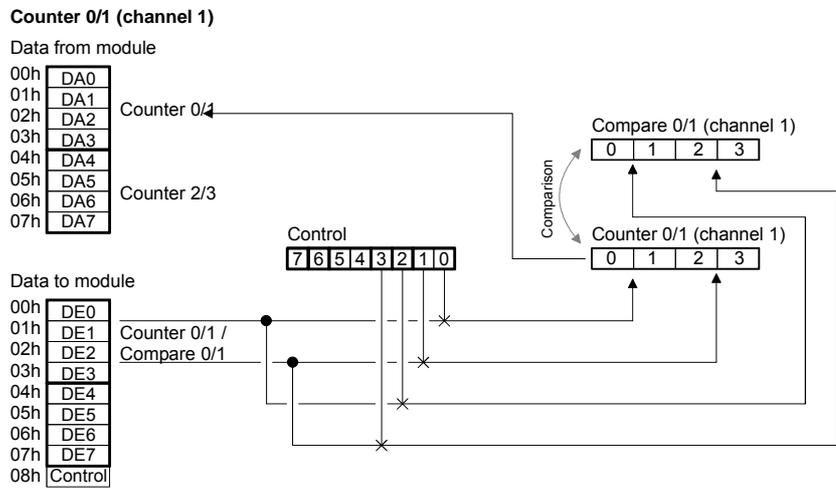
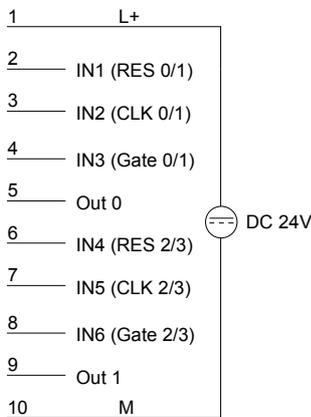


**Mode 26**  
**One Shot, count down, with reset signal**

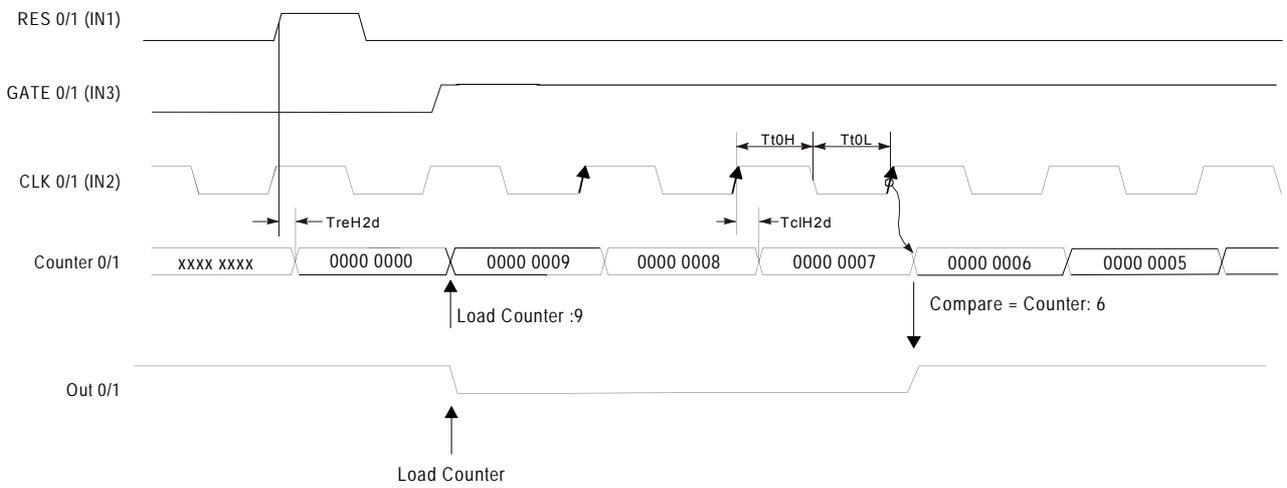
In mode 26 you may implement one 32Bit counter per channel, each one controlled by the signal applied to the GATE input. Every rising edge of the input clock decrements the counter by 1 as long as the signal applied to GATE is HIGH. RES must be at a LOW level. A HIGH level at this input would clear the counter. The counter is started by loading. Starting the counter, the output OUT is set active (LOW). OUT becomes HIGH when the value entered into COMPARE is reached.

**Mode 26 - One Shot, down, Reset**

**Pin assignment access to counter**



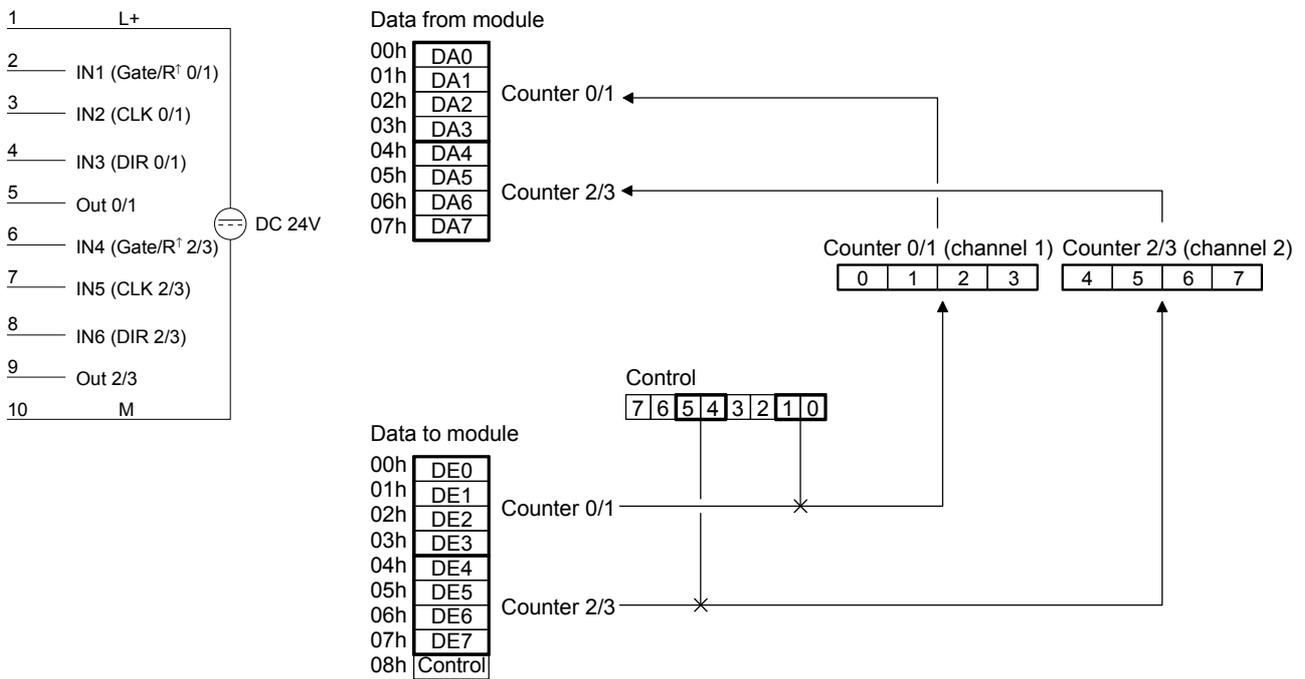
**Timing diagram** Example of counter 0/1 in mode 26:



**Mode 27**  
**32Bit counter**

You determine the direction by means of the DIR input (IN3 or IN6). Every rising or falling edge of the input clock signal increments or decrements the counter. The rising edge of the signal Gate/R<sup>↑</sup> resets the counter. During the count process, the signal Gate/R<sup>↑</sup> has to be HIGH. When the signal Gate/R<sup>↑</sup> becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter should continue counting. If the counter stops at zero, the output remains active.

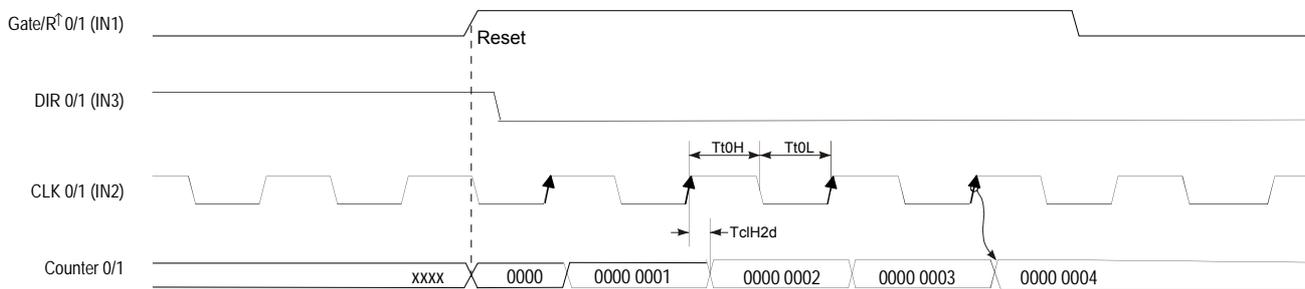
**Pin assignment**  
**access to counter**



**Up counter**

In mode 27, a LOW level at the DIR input configures the counter for counting up.

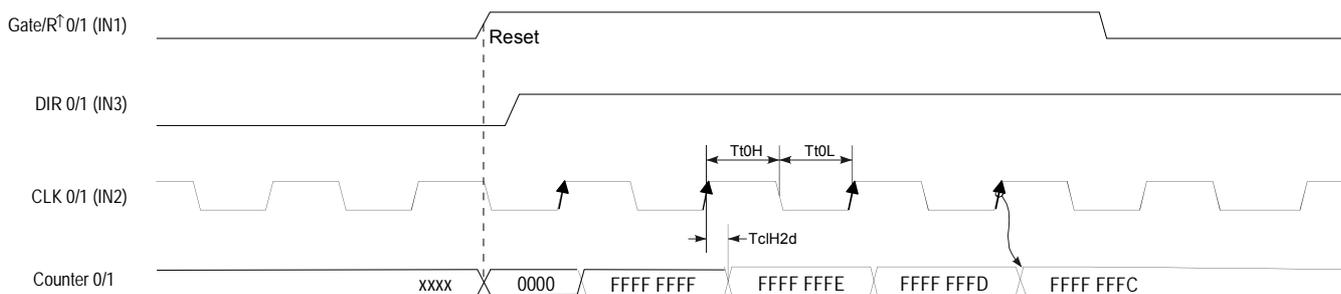
Timing diagram of the counter 0/1 example:



**Down counter**

In mode 27, a HIGH level at the DIR input configures the counter for counting down.

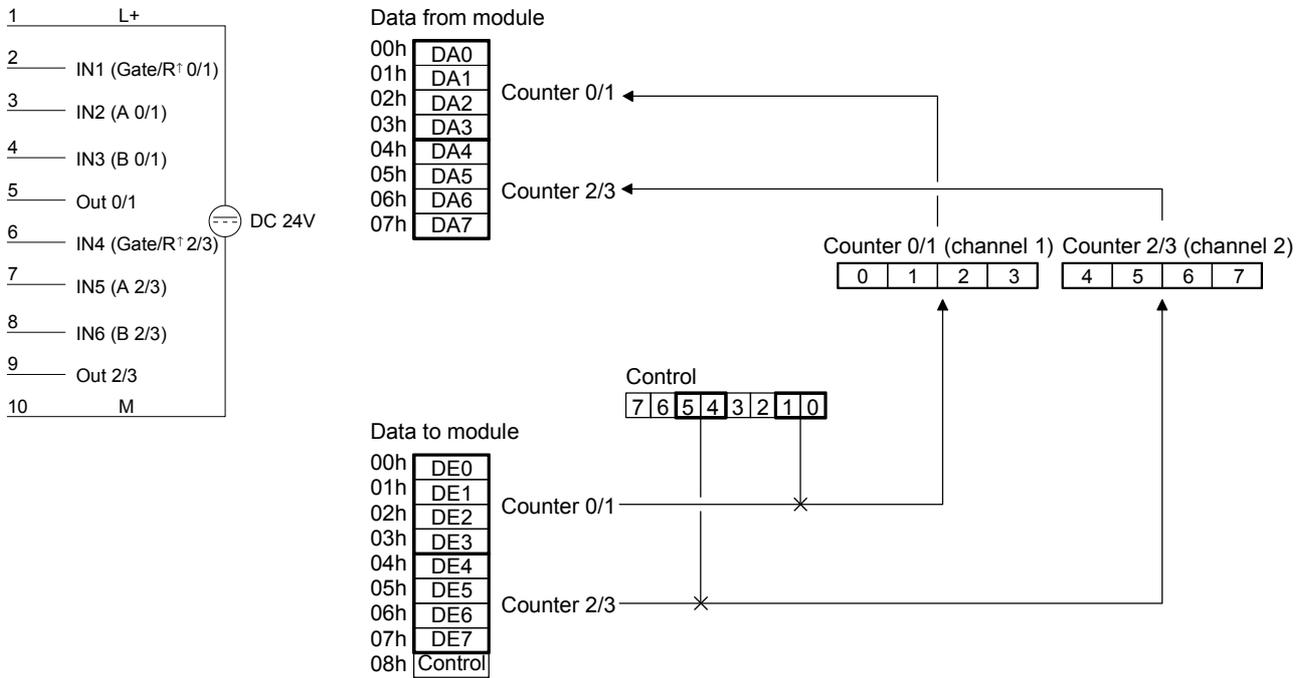
Timing diagram of the counter 0/1 example:



**Mode 28  
Encoder 1 edge**

In mode 28 you may configure an encoder for one of the channels. Depending on the direction of rotation this encoder will increment or decrement the internal counter with every falling edge. The rising edge of the signal Gate/R<sup>↑</sup> resets the counter. During the count process, the signal Gate/R<sup>↑</sup> has to be HIGH. When the signal Gate/R<sup>↑</sup> becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero the output remains active.

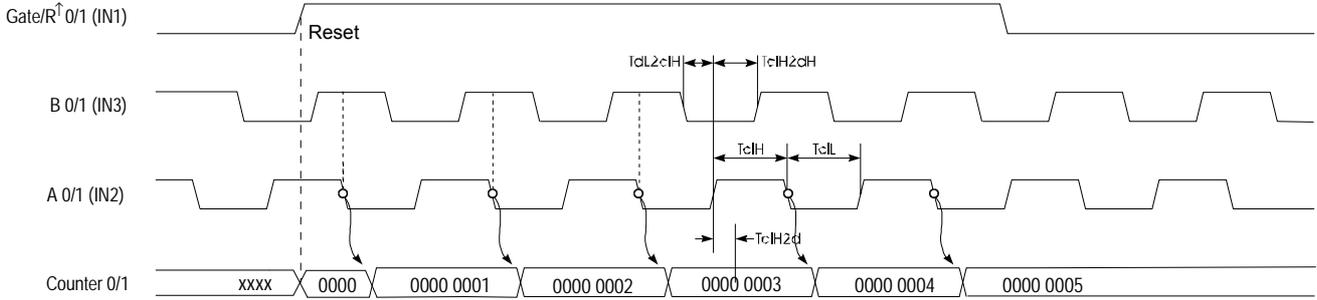
**Pin assignment  
access to counter**



**Up counter**

Every falling edge of the signal at input A increments the counter if input B is at HIGH level at this moment.

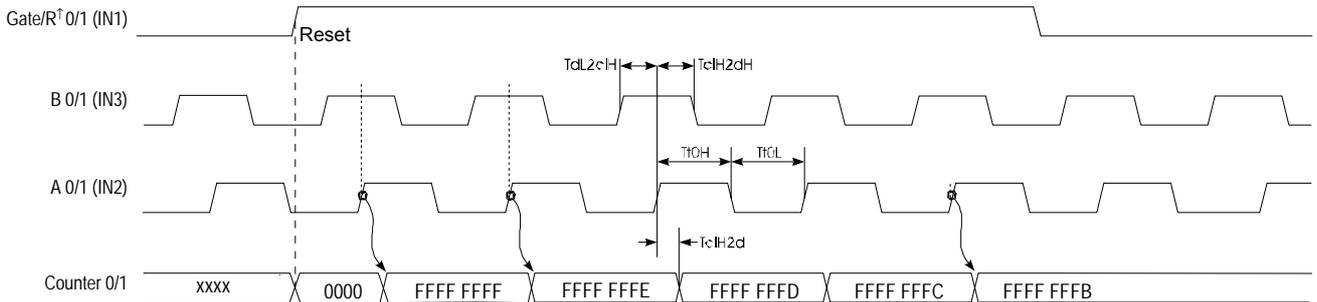
Timing diagram for the counter 0/1 example:



**Down counter**

Every rising edge of the signal at input A decrements the internal counter if input B is at HIGH level at this moment.

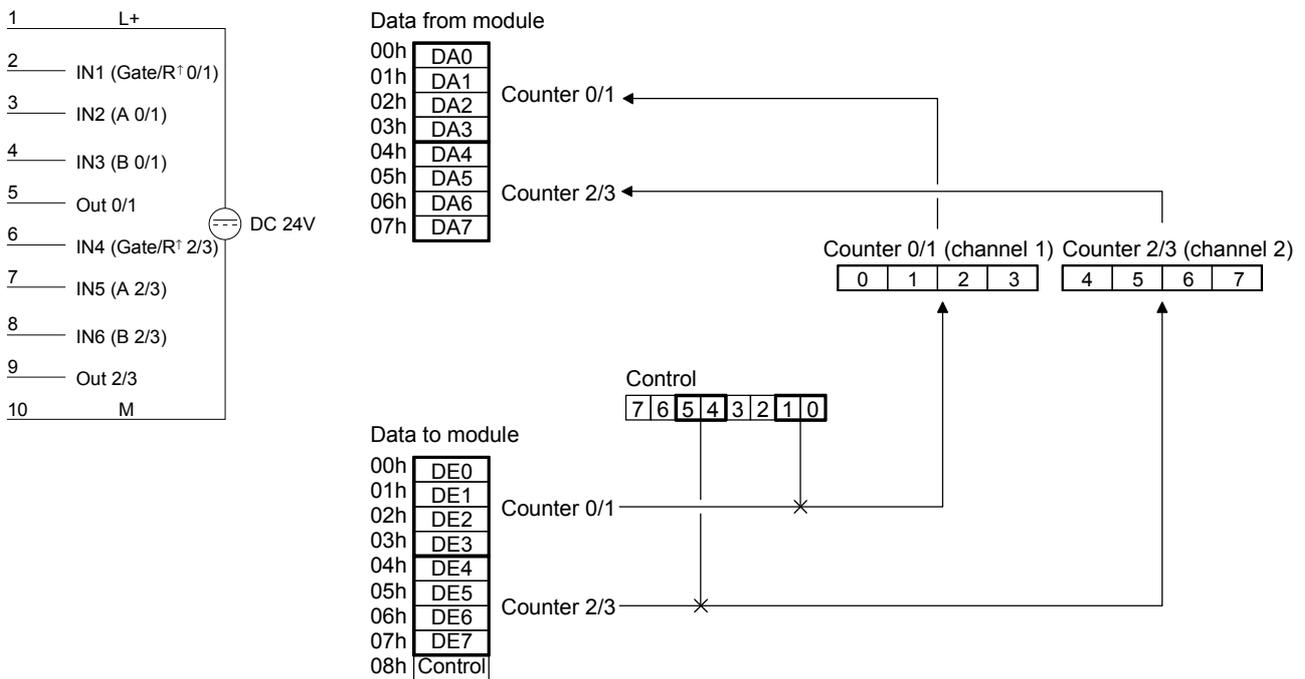
Timing diagram for the counter 0/1 example:



**Mode 29  
Encoder 2 edges**

Every rising or falling edge of the signal at input A changes the counter by 1. The direction of the count depends on the level of the signal applied to input B. The rising edge of the signal Gate/R<sup>↑</sup> resets the counter. During the count process, the signal Gate/R<sup>↑</sup> has to be HIGH. When the signal Gate/R<sup>↑</sup> becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero the output remains active.

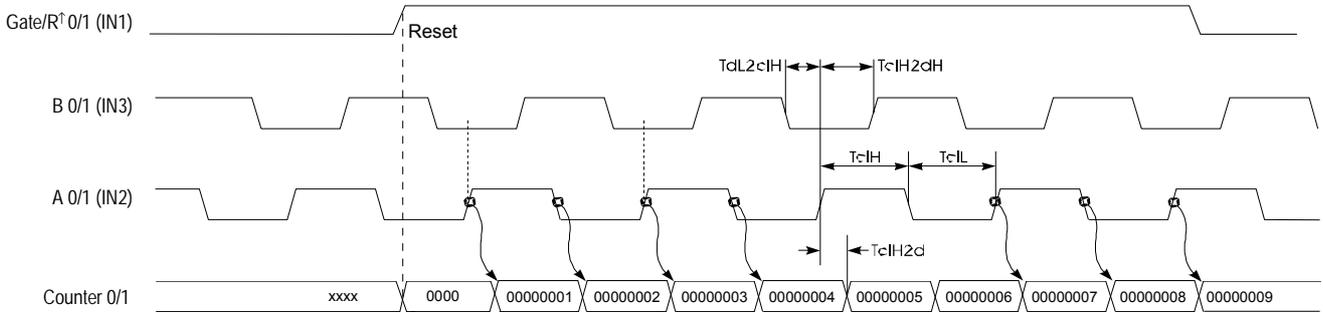
**Pin assignment  
access to counter**



**Up counter**

The counter is incremented by the rising edge of signal A if input B is at a LOW level or by the falling edge of input A when input B is at a HIGH level.

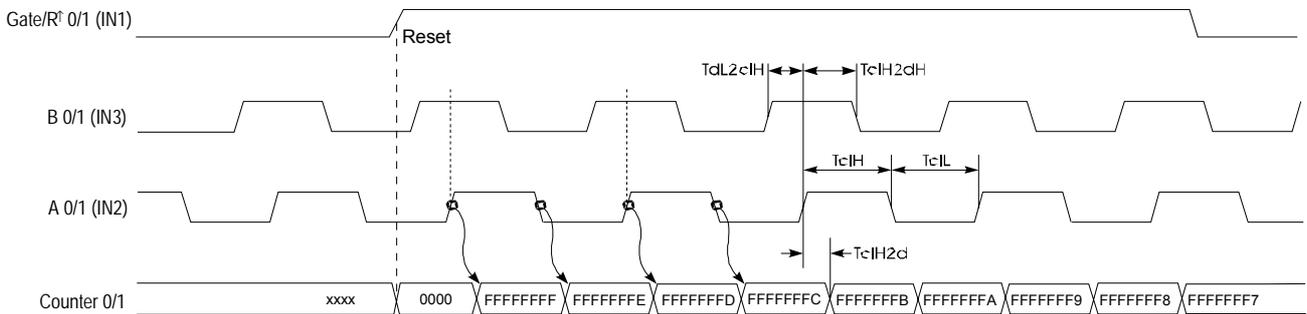
Timing diagram for the counter 0/1 example:



**Down counter**

The counter is decremented by the rising edge of signal A if input B is at a HIGH level or by the falling edge of input A when input B is at a LOW level.

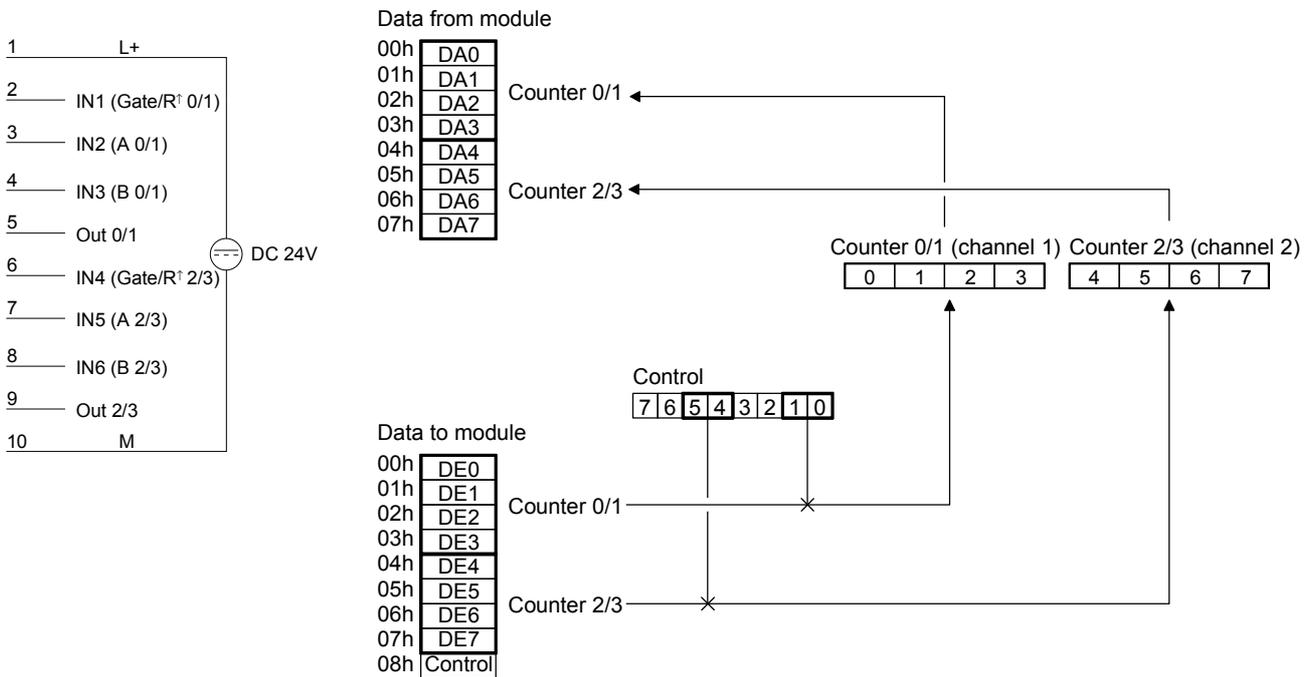
Timing diagram for the counter 0/1 example:



**Mode 30  
Encoder 4 edges**

Every rising or falling edge at inputs A or B increments or decrements the counter. The direction depends on the level applied to the other input (B or A). The rising edge of the signal Gate/R<sup>↑</sup> resets the counter. During the count process, the signal Gate/R<sup>↑</sup> has to be HIGH. When the signal Gate/R<sup>↑</sup> becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero, the output remains active.

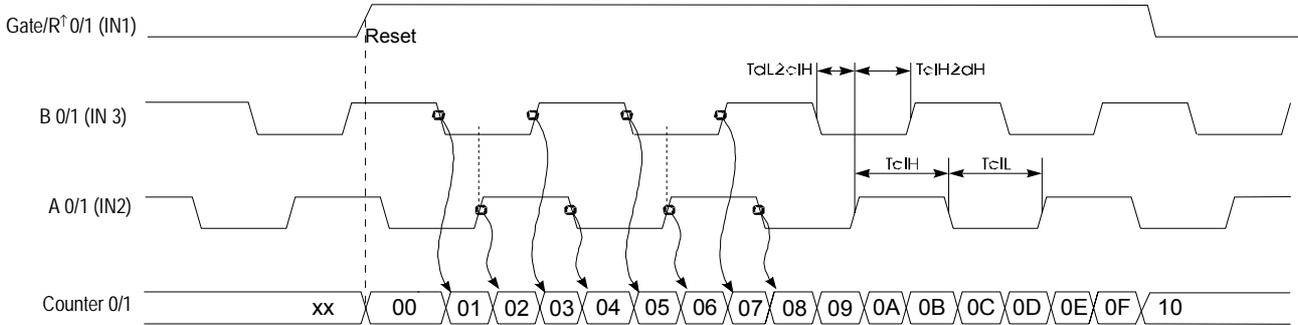
**Pin assignment  
access to counter**



**Up counter**

The counter is incremented when a rising edge is applied to B while input A is at a HIGH level or if a falling edge is applied to B when input A is at a LOW level. Alternatively it is also incremented when a rising edge is applied to A when input B is at a LOW level or by a falling edge at A when input B is at a HIGH level.

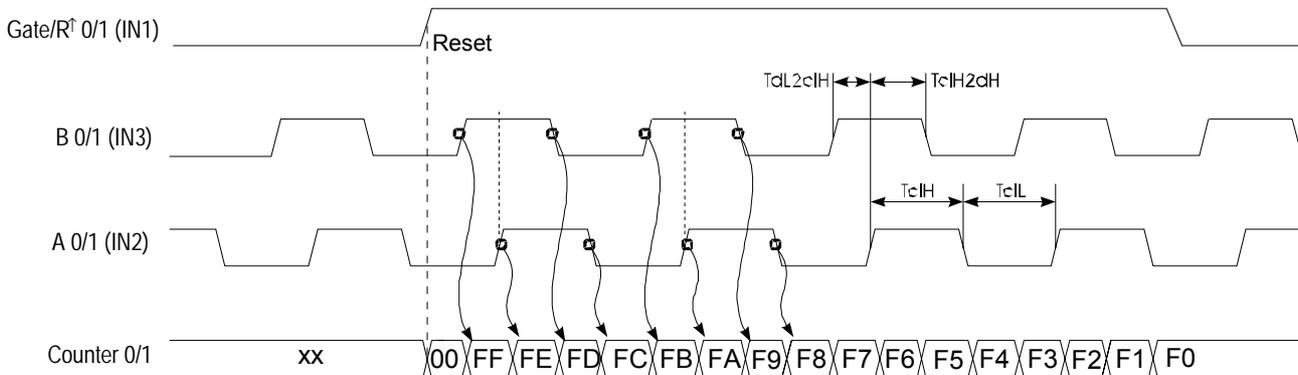
Timing diagram for the counter 0/1 example:



**Down counter**

The counter is decremented when a rising edge is applied to B while input A is at a LOW level or if a falling edge is applied to B when input A is at a HIGH level. Alternatively it is also decremented when a rising edge is applied to A when input B is at a HIGH level or by a falling edge at input A when input B is at a LOW level.

Timing diagram for counter 0/1 example:



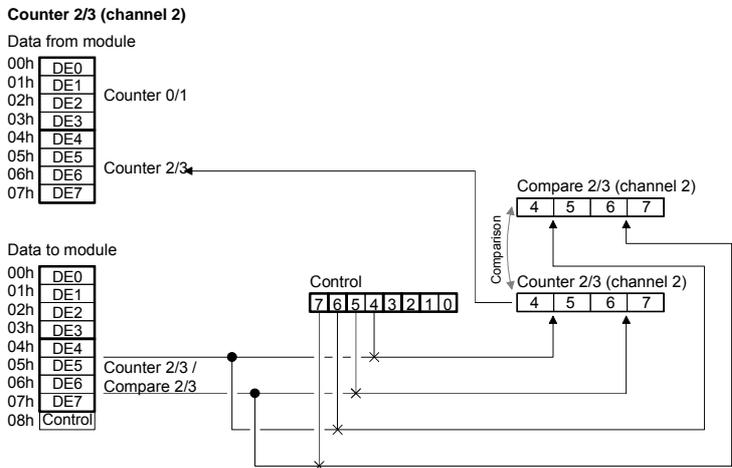
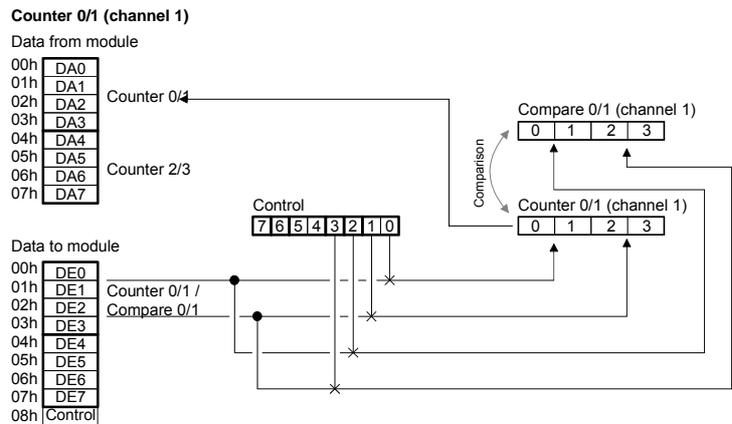
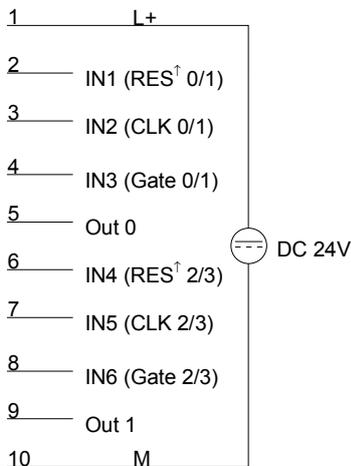
**Mode 31 and 32  
32bit counter with  
gate**

In mode 31 and mode 32 you can implement a 32Bit counter that is controlled by a gating signal (Gate). The direction of counting depends on the selected mode. Every rising edge of the input signal increments or decrements the counter provided that the GATE signal is at HIGH level. A rising edge of RES<sup>↑</sup> clears the counter. When the counter reaches the value that was previously loaded into the compare register, output OUT is set active for a minimum period of 100ms while the counter continues counting.

**Mode 31 - 32Bit counter up + gate with compare**

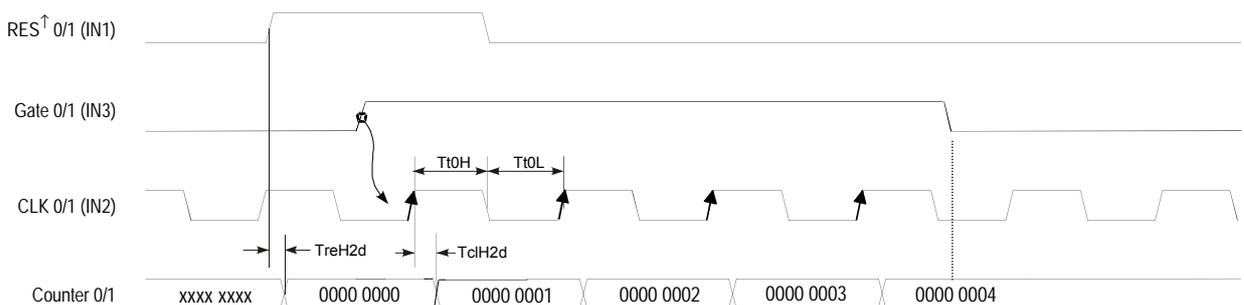
**Mode 32 - 32Bit counter down + gate with compare**

**Pin assignment  
access to counter**



**Timing diagram**

Below follows an example of a timing diagram of counter 0/1 in mode 31:



**Mode 33 and 34  
32Bit counter with  
gate and auto  
reload**

Modes 33 and 34 operate in the same manner as mode 31 and 32 with the addition of an Auto Reload function. The "Auto Reload" is used to define a value in the load register that is used to preset the counter automatically when it reaches the compare value.

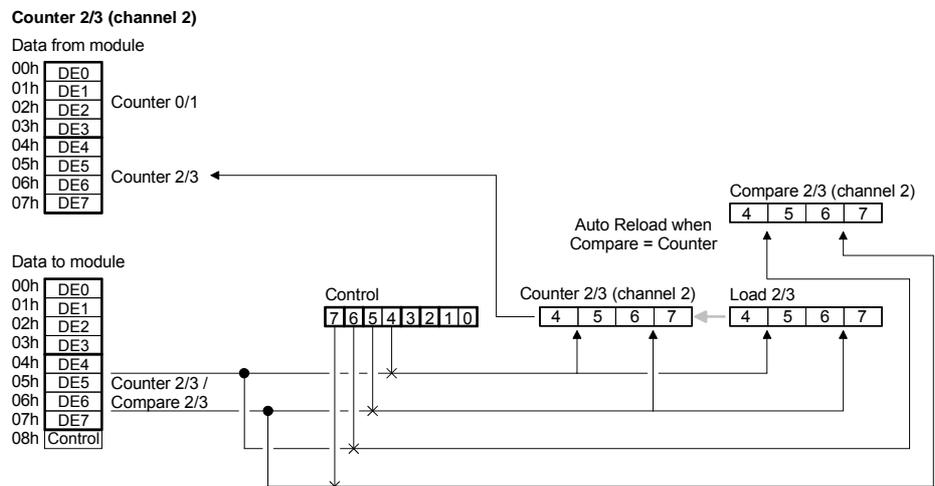
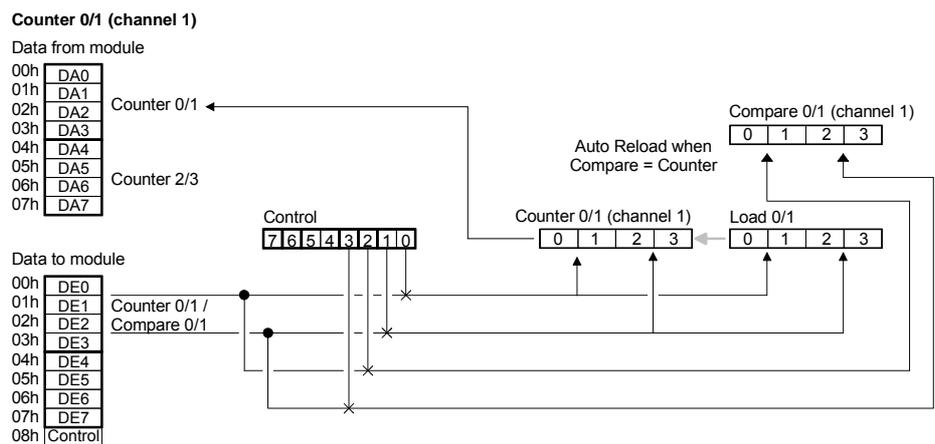
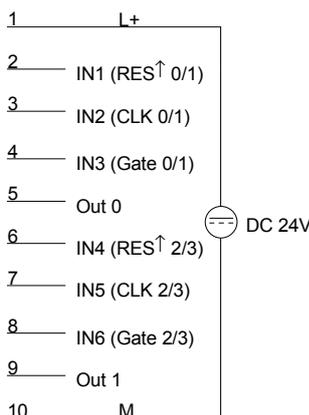
A rising edge of RES<sup>↑</sup> clears the counter to 0000 0000. A HIGH level applied to GATE enables the counter so that is incremented/decremented by every rising edge of the CLK signal. As long as GATE is HIGH, the counter will count every rising edge of the signal applied to CLK until the count is one less than the value entered into COMPARE. The next pulse overwrites the counter with the value contained in the load register. This process continues until GATE is set to a LOW level. When an auto reload occurs, the status of the respective output changes.

The RES<sup>↑</sup> signal only resets the counter but not the outputs.

**Mode 33 - 32Bit counter up + gate with compare and auto reload**

**Mode 34 - 32Bit counter down + gate with compare and auto reload**

**Pin assignment  
access to counter**



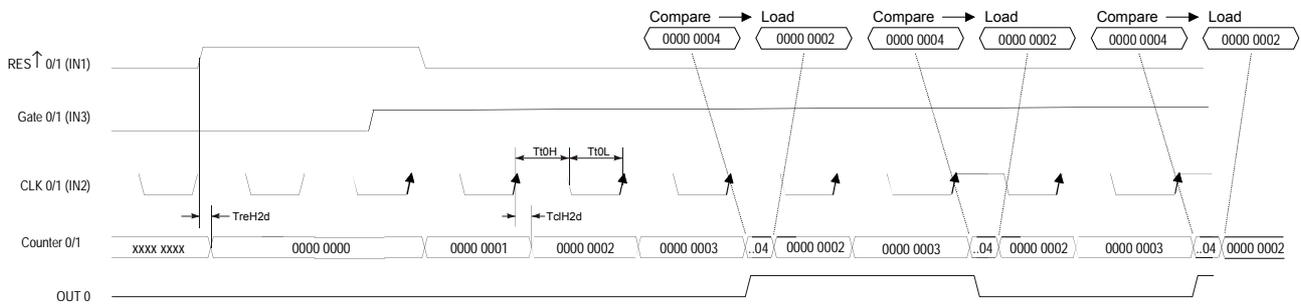
**Example**

This example is intended to explain the operation of the counters in mode 33 and 34.

A rising edge of RES<sup>↑</sup> clears the counter to 0000 0000. A HIGH level applied to GATE enables the counter. As long as GATE is HIGH the counter will count every rising edge of the signal applied to CLK until the count is one less than the value entered into COMPARE. In this example the counter counts to 0000 0004 followed immediately by an auto reload, i.e. the counter is preset to the contents of the load register (in this case 0000 0002). The state of output OUT 0 changes every time an auto reload is executed.

In this example the counter counts from 0000 0002 to 0000 0004 as long as the GATE input is at a HIGH level.

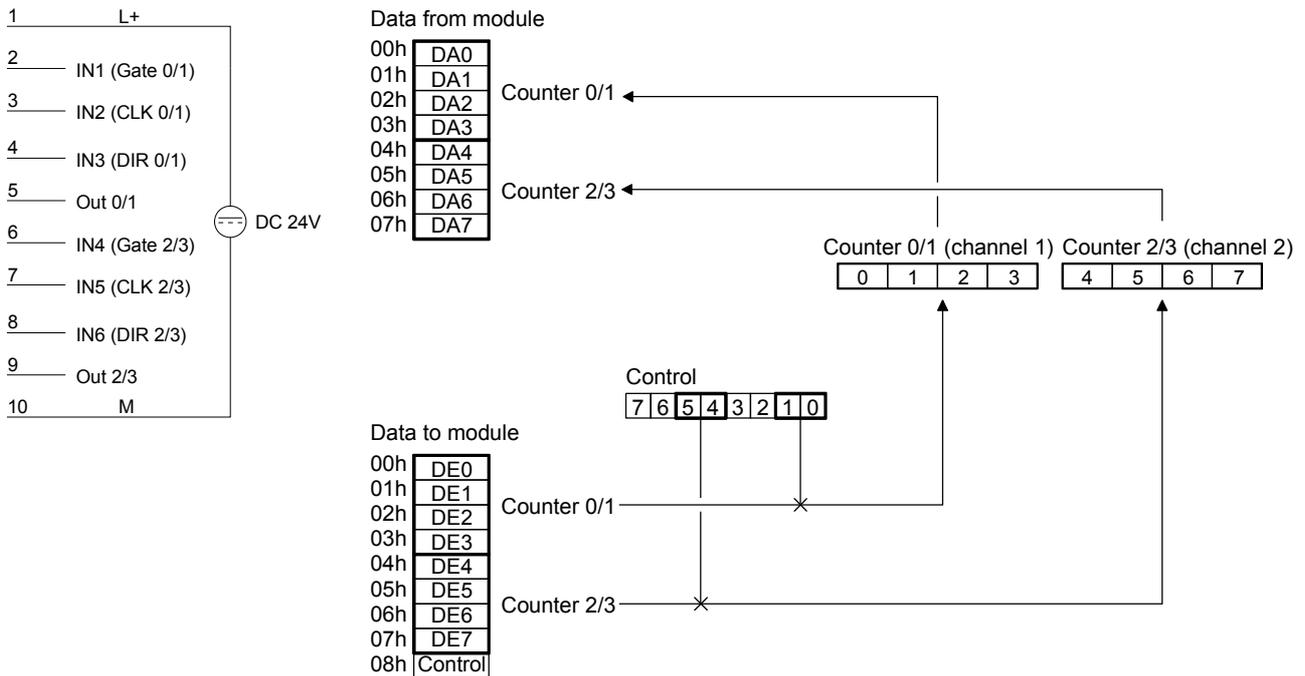
Every load operation changes the status of output OUT 0.



**Mode 35  
32Bit counter**

You determine the direction by means of the DIR input (IN3 or IN6). Every rising or falling edge of the input clock signal increments or decrements the counter. During the count process, the signal Gate has to be HIGH. When the signal Gate becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter should continue counting. If the counter stops at zero, the output remains active.

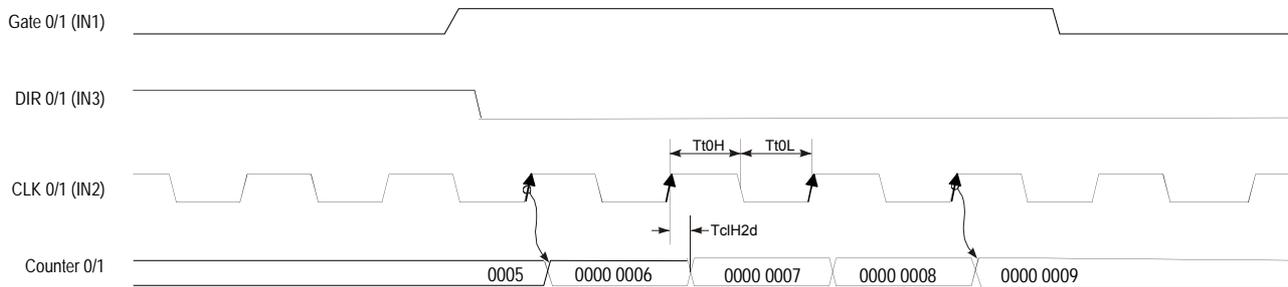
**Pin assignment  
access to counter**



**Up counter**

In mode 35, a LOW level at the DIR input configures the counter for counting up.

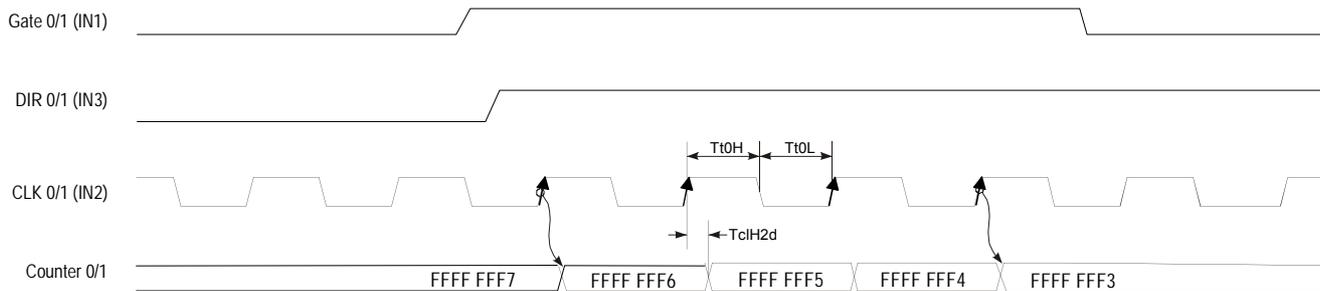
Timing diagram of the counter 0/1 example:



**Down counter**

In mode 35, a HIGH level at the DIR input configures the counter for counting down.

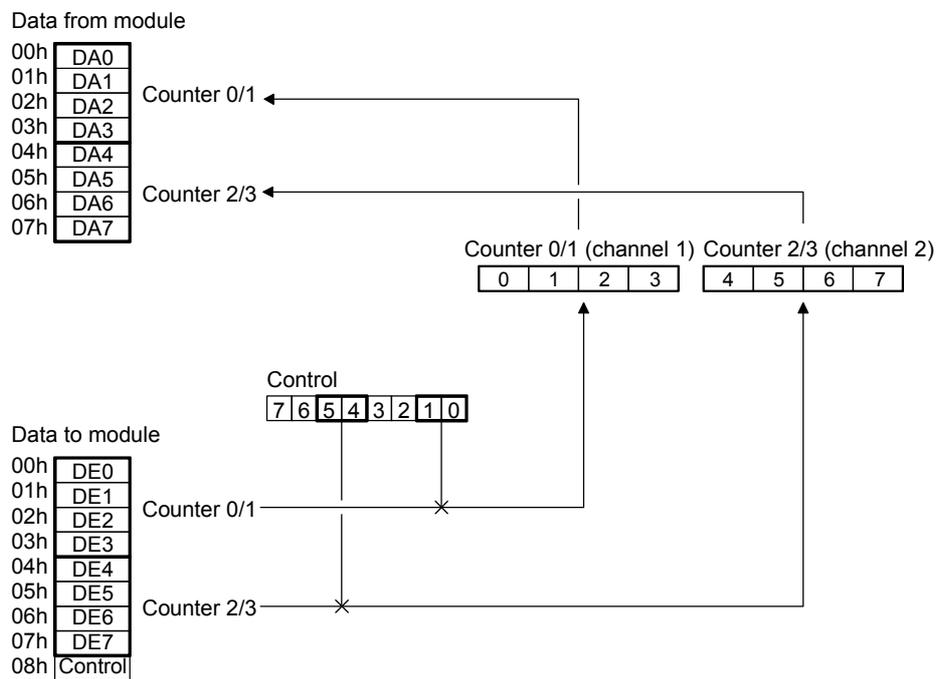
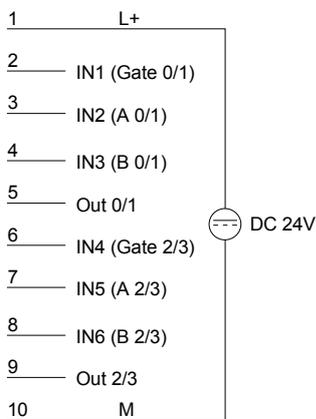
Timing diagram of the counter 0/1 example:



**Mode 36  
Encoder 1 edge**

In mode 36 you may configure an encoder for one of the channels. Depending on the direction of rotation this encoder will increment or decrement the internal counter with every falling edge. During the count process, the signal Gate has to be HIGH. When the signal Gate becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero the output remains active.

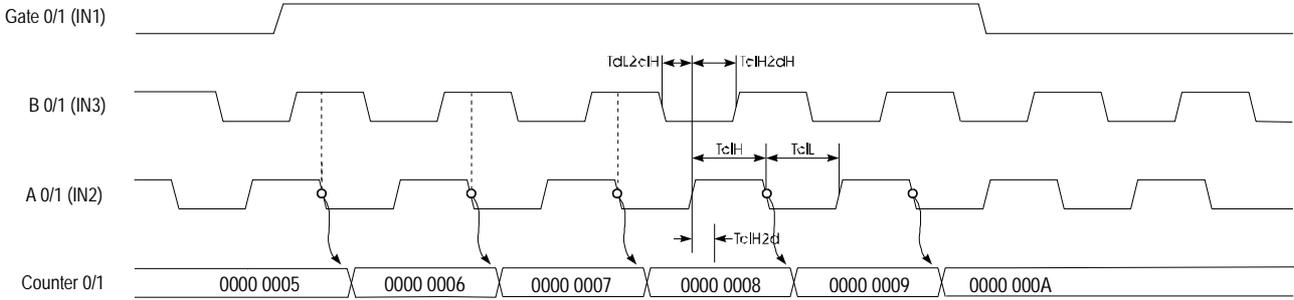
**Pin assignment  
access to counter**



**Up counter**

Every falling edge of the signal at input A increments the counter if input B is at HIGH level at this moment.

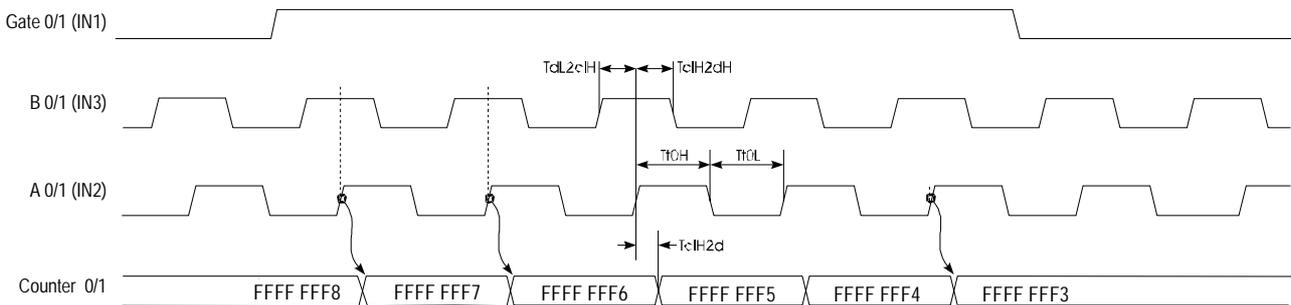
Timing diagram for the counter 0/1 example:



**Down counter**

Every rising edge of the signal at input A decrements the internal counter if input B is at HIGH level at this moment.

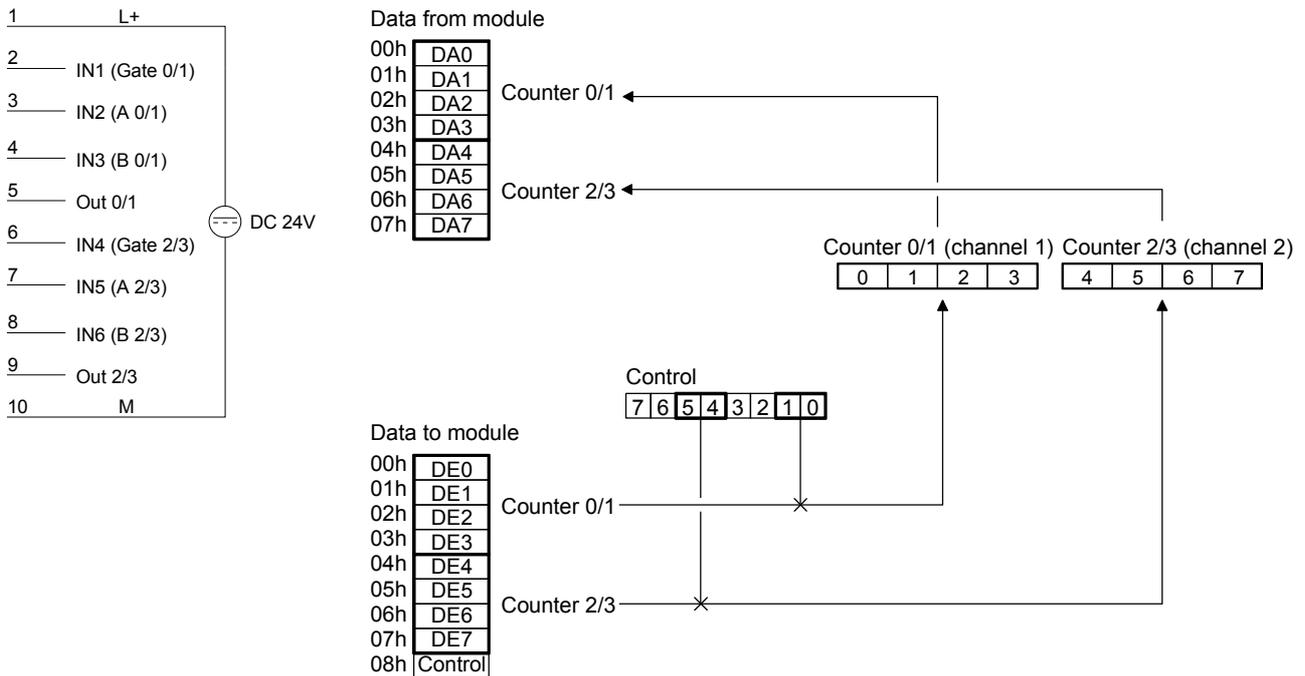
Timing diagram for the counter 0/1 example:



**Mode 37  
Encoder 2 edges**

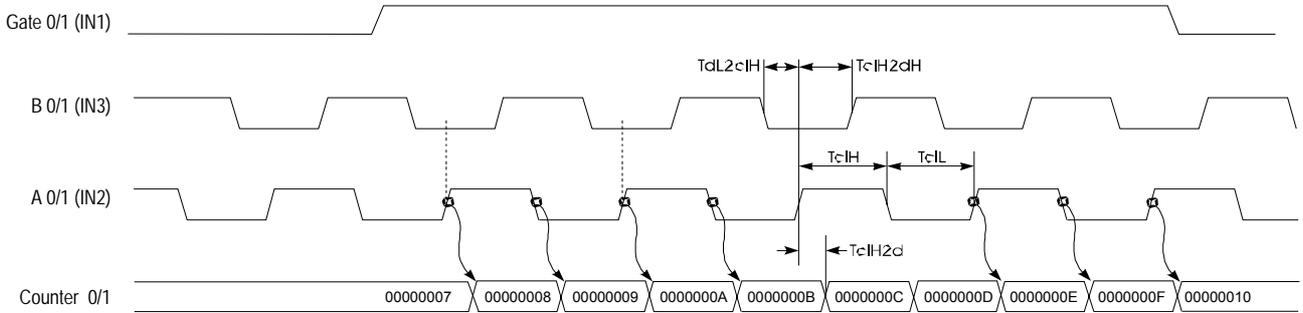
Every rising or falling edge of the signal at input A changes the counter by 1. The direction of the count depends on the level of the signal applied to input B. During the count process, the signal Gate has to be HIGH. When the signal Gate becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero the output remains active.

**Pin assignment  
access to counter**



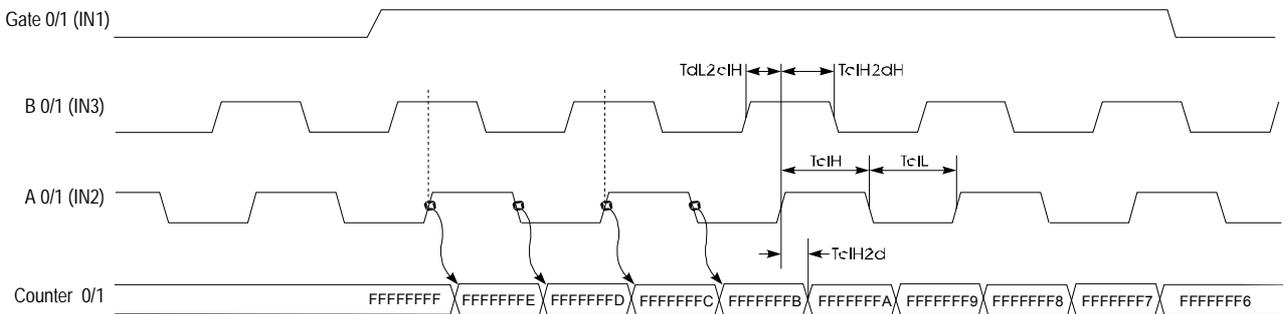
**Up counter**

The counter is incremented by the rising edge of signal A if input B is at a LOW level or by the falling edge of input A when input B is at a HIGH level.  
 Timing diagram for the counter 0/1 example:



**Down counter**

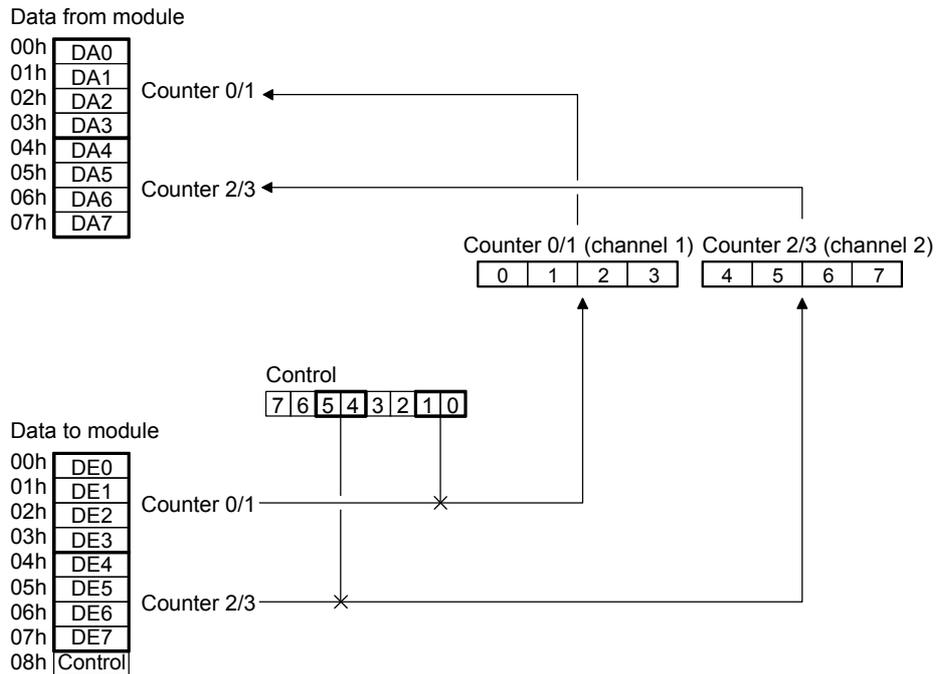
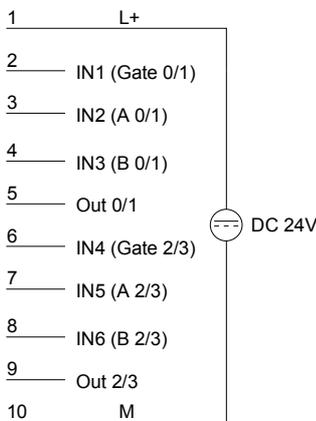
The counter is decremented by the rising edge of signal A if input B is at a HIGH level or by the falling edge of input A when input B is at a LOW level.  
 Timing diagram for the counter 0/1 example:



**Mode 38  
Encoder 4 edges**

Every rising or falling edge at inputs A or B increments or decrements the counter. The direction depends on the level applied to the other input (B or A). During the count process, the signal Gate has to be HIGH. When the signal Gate becomes "0", the counter value remains valid. When the counter reaches zero, output OUT of the respective counter is active for a minimum period of 100ms, even if the counter continues counting. If the counter stops at zero, the output remains active.

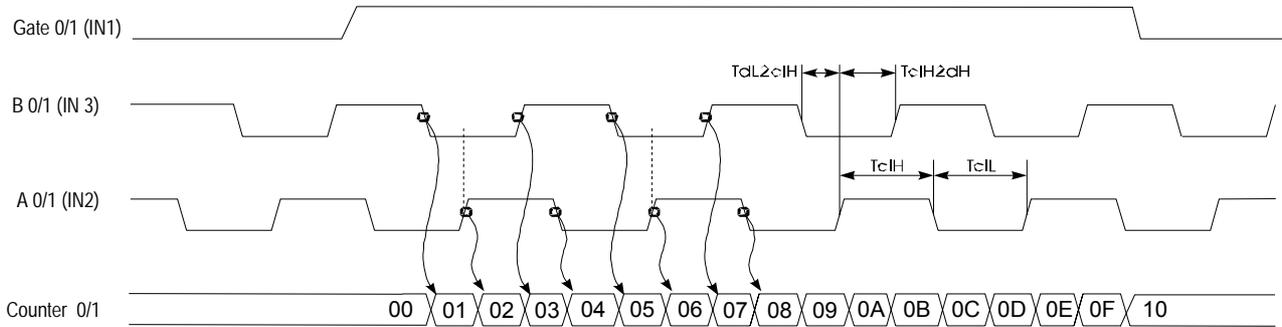
**Pin assignment  
access to counter**



**Up counter**

The counter is incremented when a rising edge is applied to B while input A is at a HIGH level or if a falling edge is applied to B when input A is at a LOW level. Alternatively it is also incremented when a rising edge is applied to A when input B is at a LOW level or by a falling edge at A when input B is at a HIGH level.

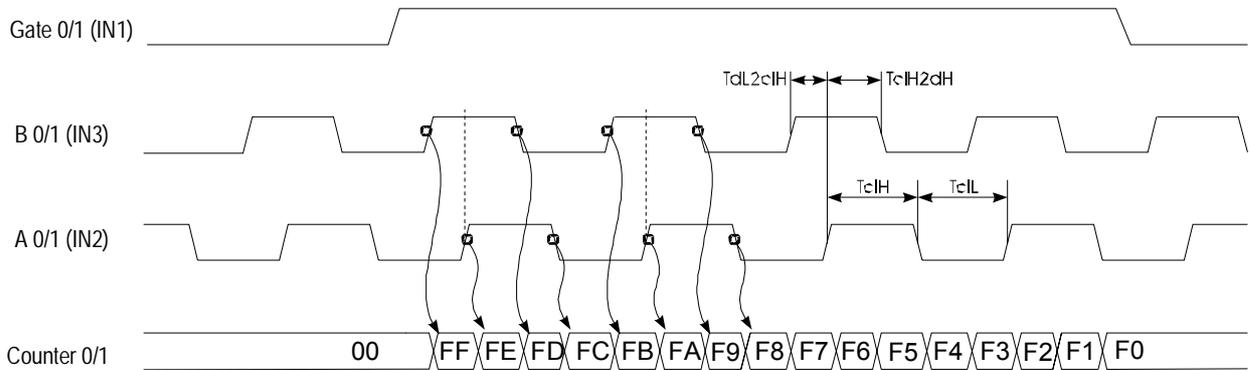
Timing diagram for the counter 0/1 example:



**Down counter**

The counter is decremented when a rising edge is applied to B while input A is at a LOW level or if a falling edge is applied to B when input A is at a HIGH level. Alternatively it is also decremented when a rising edge is applied to A when input B is at a HIGH level or by a falling edge at input A when input B is at a LOW level.

Timing diagram for counter 0/1 example:



**Mode 39 ... 42**

**Mode 39 - 32Bit Counter up + Gate low active**

**Mode 40 - 32Bit Counter down + Gate low active**

**Mode 41 - 32Bit Counter up + Gate high active**

**Mode 42 - 32Bit Counter down + Gate high active**

The modes 39 to 42 allow you to realize a 32Bit counter for each channel that is controlled via a low or high active gate signal (gate) and counts with an internal reference frequency.

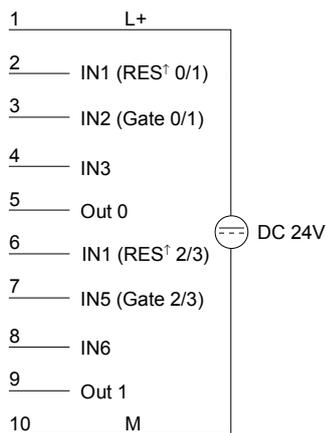
The direction of counting depends on the selected mode. With rising edge of the pulse frequency the counter is incremented res. decremented by 1.

The rising edge of the signal RES<sup>↑</sup> resets the counter.

Fref is programmable.

The OUT signal is not changed.

**Pin assignment  
access to counter**



Data from module

00h	DA0
01h	DA1
02h	DA2
03h	DA3
04h	DA4
05h	DA5
06h	DA6
07h	DA7

Counter 0/1 ←

Counter 2/3 ←

Counter 0/1 (channel 1)

Counter 2/3 (channel 2)

0	1	2	3
---	---	---	---

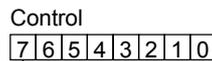
4	5	6	7
---	---	---	---

Data to module

00h	
01h	
02h	
03h	DE3
04h	
05h	
06h	
07h	DE7
08h	Control

Counter 0/1 \*

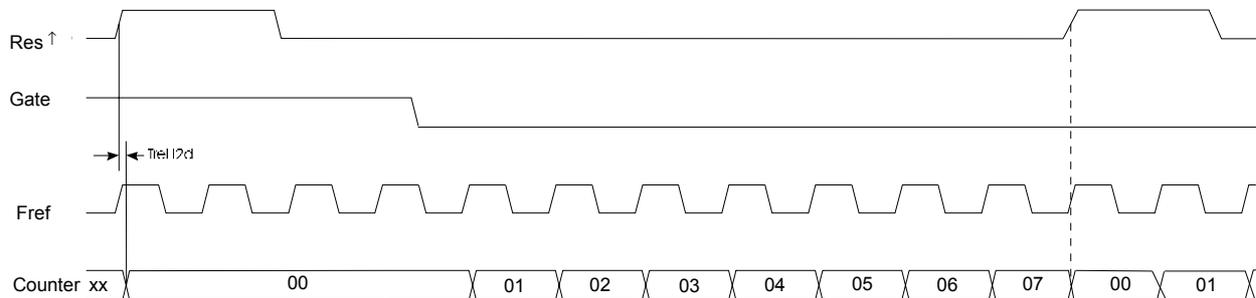
Counter 2/3 \*



Parameter  
Reference frequency  
0 : 10 MHz  
1 : 1 MHz  
2 : 100 kHz  
3 : 10 kHz

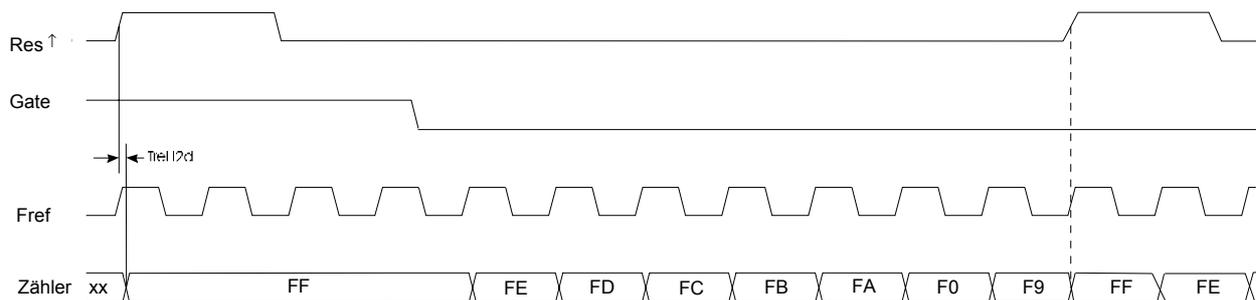
**Mode 39 32Bit Counter up + Gate low active**

The rising edge of the signal RES<sup>↑</sup> resets the counter. With the signal gate "0", the counter counts up with Fref.



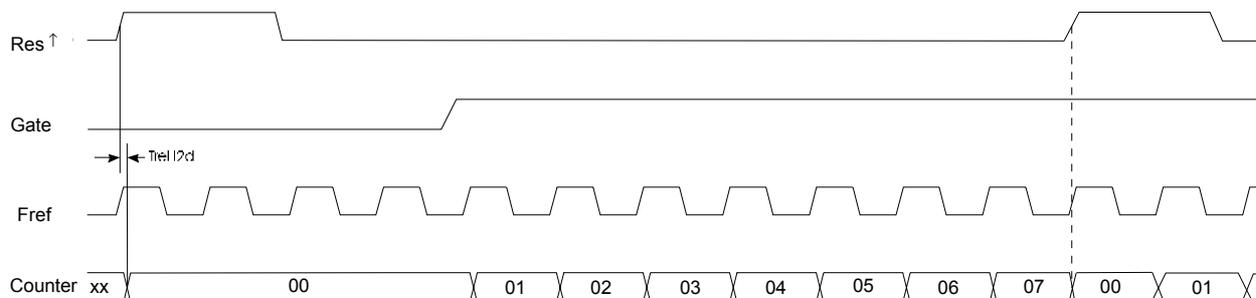
**Mode 40 32Bit Counter down + Gate low active**

The rising edge of the signal RES<sup>↑</sup> resets the counter. With the signal gate "0", the counter counts down with Fref.



**Mode 41 32Bit Counter up + Gate high active**

The rising edge of the signal RES<sup>↑</sup> resets the counter. With the signal gate "1", the counter counts up with Fref.



**Mode 42 32Bit Counter down + Gate high active**

The rising edge of the signal RES<sup>↑</sup> resets the counter. With the signal gate "1", the counter counts down with Fref.

